2025 Silicon Nanoelectronics Workshop 2025

June 8th-9th, 2025

Rihga Royal Hotel, Kyoto, Japan

Sunday, June 8th, 2025

8:30 Opening remarks

Kuniyuki Kakushima (Institute of Science Tokyo)

Session 1: Plenary Talks

Session Chair: Kuniyuki Kakushima (Institute of Science Tokyo)

8:40 1-01 (Plenary 1)

Amorphous Oxide Semiconductors for Memory Applications

Hideo Hosono (Institute of Science Tokyo & National Institute of Materials Science, Japan)

9:10 1-02 (Plenary 2)

Engineering High Quality Qubits in Silicon with Atomic Precision

Michelle Y. Simmons (Silicon Quantum Computing & University of New South Wales, Australia)

9:40-9:50 Break

Session 2: Stacked Architecture and 3D Integration

Session Chairs: Katsuhiro Tomioka (Hokkaido University) & Masaharu Kobayashi (The University of Tokyo)

9:50 2-01 (Oral 1)

First Realization of ALD based Sn-Doped InGaZnO with Reliability Enhancements for Monolithic 3D Integration

Sung-Hun Kim[1], Sun Hong Choi[1], Kota Sakai[1], Takuya Saraya[1], Toshiro Hiramoto[1], and Masaharu Kobayashi[1,2] ([1]Institute of Industrial Science, The University of Tokyo, [2]d.lab, The University of Tokyo, Japan)

10:10 2-02 (Oral 2)

Optimizing CFET Parasitic Capacitance and Performance Through Middle Dielectric Isolation and Middle Via Integration

Meng-Lin Wu[1], Yu-Cheng Lu[2], and Vita Pi-Ho Hu[1,2] ([1]Graduate Institute of Electronics Engineering, National Taiwan University, [2]Graduate School of Advanced Technology, National Taiwan University, Taiwan)

10:30 2-03 (Oral 3)

Controlling phosphorus doping at the nanoscale to promote synthetic spin orbit coupling in silicon

Michele Perego[1], Stefano Kuschlan[1], Francesc Perez-Murano[2], Jordi Llobet[2], Marta Fernandez-Regulez[2], Riccardo Chiarcos[3], Michele Laus[3], Gabriele Seguini[1], Andrea Pulici[1], Graziella Tallarida[1] ([1]CNR-IMM, Unit of Agrate Brianza, Italy, [2]Institute of Microelectronics of Barcelona, Spain, [3]Università del Piemonte Orientale "A. Avogadro", Italy)

10:50-11:00 Break

Session 3: Silicon Quantum Devices

Session Chairs: Takahide Oya (Yohokama National University) & Pei-Wen Li (National Yang Ming Chiao Tung University (NYCU))

11:00 3-01 (Invited 1)

Room Temperature Dopant-Atom Quantum Dot Transistors in Silicon

Zahid Durrani[1] ([1]Imperial College London, UK)

11:25 3-02 (Oral 4)

Experimental Demonstration of Vertically Stacked Parallel Silicon Quantum Dots

Daiki Futagi[1], Junoh Kim[1], Tomoko Mizutani[1], Takuya Saraya[1], Hiroshi Oka[2], Takahiro Mori[2], Masaharu Kobayashi[1,3], Toshiro Hiramoto[1] ([1]IIS, The Univ. of Tokyo, [2]AIST, [3]d.lab, The Univ. of Tokyo, Japan)

11:45 3-03 (Oral 5)

Parallel Silicon Single-Electron Pumps for Generating Nanoampere Current

Gento Yamahata[1], Takase Shimizu[1], Katsuhiko Nishiguchi[1], Akira Fujiwara[1] ([1]NTT Basic Research Laboratories, Japan)

12:05 3-04 (Oral 6)

High-Temperature Single-Electron Tunneling Through P-donors Affected by Confinement

Pooja Sudha[1], Soumya Chakraborty[1], Daniel Moraru[2], Arup Samanta[1] ([1]Indian Institute of Technology Roorkee (India), [2]Research Institute of Electronics, Shizuoka University, Japan)

12:25-13:30 Lunch break

Session 4: Advanced Logic and Memory Devices

Session Chairs: Steve Chung (National Yang Ming Chiao Tung University (NYCU)) & Kasidit Toprasertpong (The University of Tokyo)

13:30 4-01 (Invited 2)

High-Performance BEOL-Compatible ALD-IGZO Top-Gate Radio-Frequency Transistors

Yanqing Wu[1], Shenwu Zhu[1], Qianlan Hu[1], Anyu Tong[1] (Peking University, China)

13:55 4-02 (Oral 7)

Vertical Channel Transistor-Based OS-Si Hybrid Gain Cell for High-Density and High-Retention Embedded DRAM

Yu-Hsuan Chuang[1], Vita Pi-Ho Hu[1] ([1]National Taiwan University, Taiwan)

14:15 4-03 (Oral 8)

Below 10A CMOS-Double CFETs with Dielectric-wall-stress by Isolation-last Process for 0.0069 um^2 of SRAM-cell Design

Yi-Sung Chen[2], Yu-Shang Shih[2], Hao-Ming Huang[2], Ting-Kuan Ma[2], E Ray Hsieh[1] ([1]National Yang Ming Chiao Tung University, [2]National Central University, Taiwan)

14:35 4-04 (Oral 9)

RRAM-Based In-Memory Stochastic Computing for Naïve Bayes Classifiers

Haoran Wang[1], Zongwei Wang[1], Yabo Qin, Lin Bao, Yimao Cai[1] ([1]Peking Univ., China)

14:55-15:05 Break

Session 5: Memory and Related Technologies

Session Chairs: Minoru Oda (Kioxia) & Katsuhiko Nishiguchi (NTT Basic Research Laboratories)

15:05 5-01 (Oral 10)

Observation of State Change in 40nm TaOX ReRAM Cells during Read-disturb

Shota Suzuki[1], Naoko Misawa[1], Chihiro Matsui[1], and Ken Takeuchi[1]

1Dept. of Electrical Engineering and Information Systems, The University of Tokyo, Japan

15:25 5-02 (Oral 11)

Performance Evaluation of 3D 1T-nC Ferroelectric RAM Architectures

Wei-Chen Chen[1], Hang-Ting Lue[1], Keh-Chung Wang[1], and Chih-Yuan Lu[1] ([1]Macronix International Co., Ltd., Taiwan)

15:45 5-03 (Oral 12)

Thermally Stable Vertical-Stacked 1T1C FeRAM with Record 3.3 μF/cm2 CMW Based on Unified Ferroelectric-Oxide Semiconductor Stack

Xujin Song[1,2†], Dijiang Sun[1,2†], Jiajia Zhang[1,2], Chenxi Yu[1,2], Xiaoyan Liu[1,2], Jinfeng Kang[1,2*] ([1]Peking University, [2]Beijing Advanced Innovation Center for Integrated Circuits, China)

16:05 5-04 (Oral 13)

InAs/AlSb III-V NVM with High-speed (5ns) Low-power (1V) QW-tunnel Program for 10-year Storage by 2DEG-enhanced Retention

Jun Sheng Hou[1], Zi Yao Chung[2], Min Jie Chen[2], Ren Fu Ye[1], Li Cheng Chen[1], E Ray Hsieh[3,*], Jen-Inn Chyi[1] ([1]National Central Univ., [2]National Yang Ming Chiao Tung Univ., Taiwan)

16:25 5-05 (Oral 14)

A Novel Cross-Point Ferroelectric-Capacitor Array based Parallel In-Memory Encryption for Energy-Efficient Secure-AI Applications

Shengjie Cao[1], Weikai Xu[1], Zhiyuan Fu[2], Minyue Deng[1], Zebin Zhang[1], Qianqian Huang[1,3*] and Ru Huang[1,3*] ([1]Peking University, China, [2]Southeast University, China, [3]Beijing Advanced Innovation Center for Integrated Circuits, China)

16:45-17:00 Break

Session 6: Poster session with shot-gun presentations

17:00-18:30 Starting with short oral presentations (17:00~17:35)

Session Chairs: Daniel Moraru (Shizuoka University) & Katsuhiko Nishiguchi (NTT Basic Research Laboratories)

(List of posters is available at the end.)

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Monday, June 9th, 2025

Session 7: Advanced Electronics on New Materials

Session Chairs: Louis Hutin (CEA Leti) & Takahiro Shinada (Tohoku University)

8:30 7-01 (Invited 3)

Capacitor-less IGZO based gain cell (2T0C): A disruptive technology for high-density eDRAM and 3D-DRAM

Attilio Belmonte[1], Hyungrock Oh[1], Nouredine Rassoul[1], Subhali Subhechha[1], Adrian Chasin[1], Daisuke Matsubayashi[1], Yiqun Wan[1], Harold Dekkers[1], Romain Delhougne[1], Gouri Sankar Kar[1] ([1]imec, Belgium)

8:55 7-02 (Oral 15)

BEOL-Compatible IGZTO Thin-Film Transistors with Ultra-High Positive Bias Stress Stability for Advanced Electronics

Kai Chen[1,2], Xiaonan Wu[1,2], Ran Cheng[1], Rui Zhang[1], Junkang Li[1*], Yunlong Li[1,2*] ([1]Zhejiang University, China, [2]Zhejiang ICsprout Semiconductor Co., Ltd, China)

9:15 7-03 (Oral 16)

Enhanced Electrical Characteristics of Ge MOS Device by In-situ Low Temperature H_2 Treatment

Pai-Yu Hsiao[1,‡], Dun-Bao Ruan[2,‡], and Kuei-Shu Chang-Liao[1,*], Hsin-I Yeh[1], Chih-Wei Liu[1], Yu-Hsuan Chien[1], Bo-Lien Kuo[1], Kai-Chun Yang[1], Cheng-Han Li[1], Cheng-Yu Wu[1] ([1]National Tsing Hua University, Taiwan, [2]Fuzhou University, China)

9:35 7-04 (Oral 17)

Synergistic Impact of Random Phase Distribution and Polarization Strength Variations on FeFET Across Grain Sizes and Ferroelectric Percentages

Yi-Ming Tseng[1*] and Vita Pi-Ho Hu[1,2**] ([1]National Taiwan University, Taiwan, [2]National Taiwan University, Taiwan)

9:55 7-04 (Oral 18)

Unified Memcapacitor-Memristor Memory for Synaptic Weights and Neuron Temporal Dynamics

S. D'Agostino[1*], M. Massarotto[2*], T. Torchet[3], F. Moro[3], N. Castellani[1], L. Grenouillet[1], Y. Beilliard[1], D. Esseni[2], M. Payvand[3], and E. Vianello[1†] ([1]CEA, LETI, Universite Grenoble Alpes, France, [2]DPIA, Universita degli Studi di Udine, Italy, [3]University of Zurich and ETH Zurich, Switzerland)

10:15 7-05 (Oral 19)

Poly-Si Nanosheet FETs With Vertical C-Shaped Channel Using Pulse Laser Crystallization

Jinbiao Liu[1], Zhuo Chen[1], Yongkui Zhang[1], Junfeng Li[1], Xianglie Sun[2], Shujuan Mao[2], Guilei Wang[2], Chao Zhao[2], Huilong Zhu[1], and Jun Luo[1] ([1]Institute of Microelectronics, Chinese Academy of Sciences, [2]Beijing Superstring Academy of Memory, China)

10:35-10:45 Break

Session 8: Advanced CMOS Devices

Session Chairs: Hiroaki Satoh (Shizuoka Univ.) & Runsheng Wang (Peking University)

10:45 7-06 (Oral 20)

Heterojunction Tunneling and Reverse Shockley–Read–Hall Recombination Effects in $Si_{1-x}Ge_x$ Channel/Si SDE CFETs for Steeper Subthreshold Swing and Low DIBL

Pei-lun Chang, Ying-Tsan Tang* (National Central University, Taiwan)

11:05 8-02 (Oral 21)

Statistical Analysis of Subthreshold Current Distributions in bulk MOSFETs at Room and Cryogenic Temperatures

Tomoko Mizutani[1], Kiyoshi Takeuchi[1], Takuya Saraya[1], Hiroshi Oka[2], Takahiro Mori[2], Masaharu Kobayashi[1], Toshiro Hiramoto[1] ([1]Univ. of Tokyo, [2]AIST, Japan)

11:25 8-03 (Oral 22)

Investigation on Enhanced Hot Carrier Degradation in FinFETs at Cryogenic Temperature

Zirui Wang[1], Zuoyuan Dong[1,2], Hongbo Wang[1], Zixuan Sun[1], Yue-Yang Liu[3], Xing Wu[2], Runsheng Wang[1] ([1]Peking Univ., [2]East China Normal Univ., [3]Inst. of Semiconductors, China)

11:45 8-04 (Oral 23)

Study of Current Inflections in Reverse Bias in Nano-dimensional Silicon Esaki Diodes

Daris Alfafa[1,2], Arief Udhiarto[2], Daniel Moraru[1,3] ([1]Graduate School of Sci. and Tech., Shizuoka Univ. (Japan), [2]Department of Electrical Eng., Univ. of Indonesia (Indonesia), [3]Res. Inst. of Electronics, Shizuoka Univ., Japan)

12:05 8-05 (Oral 24)

Deep Learning to Automate Fitting and Parameter Extraction of 2D Transistors

Robert K. A. Bennett[1], Harmon F. Gault[1], Asir Intisar Khan[1], Lauren Hoang[1], Tara Peña[1], Kathryn Neilson[1], Young Suh Song[1], Zhepeng Zhang[2], Andrew J. Mannix[2], Eric Pop[1,2,3] ([1]Stanford Univ., Dept. of Electrical Eng., [2]Stanford Univ., Dept. of Materials Sci. & Eng., [3]Stanford Univ., Dept. of Appl. Phys., USA)

12:25-13:30 Lunch break

Session 9: Interfaces and Reliability Engineering

Session Chairs: Michele Perego (CNR-IMM) & Toshifumi Irisawa (AIST)

13:30 9-01 (Invited 4)

Charge pumping electrically-detected magnetic resonance in Si MOS transistors — Identification of interface defects and dopant atoms —

Masahiro Hori (Research Institute of Electronics, Shizuoka University, Japan)

13:55 9-02 (Oral 25)

O/H Supercritical Fluid Passivation on Stacked $Ge_{0.95}Si_{0.05}$ Nanosheet nFETs

Min-Kuan Lin[1], Ding-Wei Lin[2], Jui-Yu Hsu[2], Guan-Hua Chen[2], Bo-Hui Yu[3], Wei-Jen Chen[2], Bo-Wei Huang[2], Tao Chou[1], Yi-Chun Liu[2], Yu-Rui Chen[2], Hong-Yi Tu[4], Ting-Chang Chang[5], and C. W. Liu[1,2,3,*] ([1]Graduate School of Advanced Technology, [2]Graduate Institute of Electronics Engineering, [3]Graduate Institute of Photonics and Optoelectronics, National Taiwan University, Taipei, Taiwan, [4]Department of Materials and Optoelectronic Science, [5]Department of Physics, National Sun Yat-Sen University, Kaohsiung, Taiwan)

14:15 9-03 (Oral 26)

Total Ionizing Doses Effects on MOSFET, FinFET, and GAAFET after Co-60 Radiation Exposure

Jing-Lin Zheng[1,‡], Dun-Bao Ruan[2,‡], and Kuei-Shu Chang-Liao[1,*], Shang-Hua Hsu[1] ([1]National Tsing Hua University, Taiwan, [2]Fuzhou University, China)

14:35 9-04 (Oral 27)

Improved Uniformity and Endurance of Ag-based Volatile Memristors via Annealing Engineering

Yading Yi[1,3], Xujin Song[1,3], Zhuohua Tang[1,3], Shangze Li[1,3], Dijiang Sun[1,3], Shiyue Song[1,3], Yulin Feng[*2], Zheng Zhou[1,3], Peng Huang[1,3], Jinfeng Kang[1,3], Lifeng Liu[*1,3] ([1]Peking University; [2]Beijing Information Science and Technology University; [3]Beijing Advanced Innovation Center for Integrated Circuits, China)

14:55-15:05 Break

Session 10: Quantum-Dot Devices

Session Chairs: Gento Yamahata (NTT Basic Research Laboratories) & Daniel Moraru (Shizuoka University)

15:05 10-01 (Invited 5)

Spatial Noise Correlation in Silicon Qubit Devices

Jun Yoneda[1] ([1]Univ. of Tokyo (Japan))

15:30 10-02 (Oral 28)

Experimental Observation of Sequential Electron Incorporation within P-Donor Molecules in a Silicon Nano-Transistor

Soumya Chakraborty[1], Pooja Sudha[1], Hemant Arora[1], Daniel Moraru[2], Arup Samanta[1,3] ([1]Indian Institute of Technology Roorkee, India, [2]Res. Inst. of Electronics, Shizuoka Univ., Japan, [3]Centre of Nanotech., Indian Institute of Technology Roorkee, India)

15:50 10-03 (Oral 29)

Probing Low-Frequency Charge Noise in Few-Hole Physically-Defined Ge Quantum-Dot Single-Hole Transistors

Chi-Cheng Lai[1], Ting Tsai[1], Horng-Chih Lin[1], Pei-Wen Li[1] ([1]National Yang Ming Chiao Tung University, Taiwan)

16:10 10-04 (Oral 30)

3D Stacked Silicon Quantum Dots Using Potential Barriers by Shared Gates

Junoh Kim[1], Daiki Futagi[1], Tomoko Mizutani[1], Takuya Saraya[1], Hiroshi Oka[2], Takahiro Mori[2], Masaharu Kobayashi[1,3], Toshiro Hiramoto[1] ([1]IIS, The Univ. of Tokyo, [2]AIST, [3]d.lab, The Univ. of Tokyo, Japan)

16:30 10-05 (Oral 31)

Multiple-Electron Random Network System Simulation Based on Carbon Nanotube/Polyoxometalate Network

Shunya Watanabe[1], Takahide Oya[1] ([1]Yokohama National University, Japan)

16:50-17:00 Break

Session 11: 30th Anniversary Panel Session

17:00-18:20 Silicon Nanoelectronics and Related Trends Over the Next 30 Years

Moderator: Daniel Moraru (Shizuoka University)

18:20-18:30 Closing Remarks (Daniel Moraru & SNW2026 Team**)**

List of Poster Presentations

P1 Integration of Optimized Superlattice HfO_2/ZrO_2 Dielectric into High-Performance Superlattice SiGe/Si p-type GAAFETs

Kai-Ting Huang[1], Yi-Ju Yao[1], Heng-Jia Chang[2], Chen-You Wei[1], Yu-Min Fu[1], Bo-Xu Chen[2], Tsai-Jung Lin[1], Yung-Teng Fang[2], Guang-Li Luo[3], Fu-Ju Hou[3], Yung-Chun Wu[1,2] ([1]College of Semiconductor Research, [2]Department of Engineering and System Science, National Tsing Hua University, [3]Taiwan Semiconductor Research Institute, Taiwan)

P2 BEOL-Compatible GAAFET Hybrid Memory Based on HfO_2/ZrO_2 Superlattice with Morphotropic Phase Boundary

Kuei-Chun Liao[1], Chen-You Wei[1], Yi-Ju Yao[1], Cheng-En Wu[2], Chien-Lung Chen[2], Chih-Chao Yang[3], Guang-Li Luo[3], Fu-Ju Hou[3], Yung-Chun Wu[1,2] ([1]College of Semiconductor Research, [2]Department of Engineering and System Science, National Tsing Hua University, [3]Taiwan Semiconductor Research Institute, Taiwan)

P3 Study on the Application and Reliability of High-k HfO_2/ZrO_2 Superlattice Dielectrics in Ge Stacked Nanosheet GAAFET at 4K Ultra-Low Temperature

Kao Tsu-I[1], Huang Kai-Wei[1], Wei Chen-You[2], Lin Yi-Wen[1], Hou Fu-Ju[3], Luo Guang-Li[3], Wu Yung-Chun[1,2] ([1]Dept. of Engineering and System Science, [2]College of Semiconductor Research, National Tsing Hua Univ., Taiwan, [3]Taiwan Semiconductor Research Institute, Taiwan)

P4 Enhanced Reliability and Wake-Up Free Behavior of HfO_2/ZrO_2 Superlattice FeRAM With Triple-Level Cell Using High- and Low-Temperature ALD Stacks

Kuan-Wen Huang[1], Kun-Tao Lin[1], Yu-Yun Wang[1], Tien-Sheng Chao[1] ([1]Department of Electrophysics, National Yang Ming Chiao Tung University, Taiwan)

P5 Implementation of Delay-Enabled Axons for Lightweight Neural Networks with Improving Accuracy in Edge Computing

GuangJin Li[1,3], Hao Ai[1,3], HaoKai Guan[1,3], LiHao Zhang[1,3], YuLin Feng[2], Zheng Zhou[1,3], Peng Huang[1,3], LiFeng Liu[1,3] ([1]School of Integrated Circuits, Peking University, China, [2]Beijing Information Science and Technology University, China, [3]Beijing Advanced Innovation Center for Integrated Circuits, China)

P6 Study of Single-Photon Detection Using a Back-Gated Si Single-Electron Transistor

Shogo Miyagawa[1], Jeygopi Panisilvam[1], Pooja Sudha[2], Arup Samanta[2], Daniel Moraru[1] ([1]Research Institute of Electronics, Shizuoka Univ., Japan, [2]Department of Physics, Indian Institute of Technology Roorkee, India, [3]Centre of Nanotechnology, Indian Institute of Technology Roorkee, India)

P7 An Experimental Study on Hot-hole Injection (HHI) in Floating-gate (FG) Flash Memory

Chang Chen[1], Yang Feng[1], Jixuan Wu[1], Jing Liu[2], Junyu Zhang[3], Xuepeng Zhan[1], Jiezhi Chen[1] ([1]Shandong University, China, [2]Institute of Microelectronics of Chinese Academy of Sciences, China, [3]Neumem Co., Ltd, Hefei, China)

P8 BEOL-Compatible Annealing Effects on Properties of ALD NbO_x Films

Gaoqi Yang[1], Ruiqing Xie[1], Linbo Shan[1], Jiye Li[1], Zongwei Wang[1,2], Yimao Cai[1,2] ([1]School of Integrated Circuits, Peking University, China, [2]Beijing Advanced Innovation Center for Integrated Circuits, Peking University, China)

P9 Multi-Level Split Weight Learning for Multi-Cell ReRAM Computation-in-Memory

Rei Kusunose[1], Seiji Adachi[1], Ayane Matsuzaki[1], Takao Marukame[1], Kota Ando[1], Tetsuya Asai[1] ([1]Graduate School of Information Science and Technology, Hokkaido University, [2]Faculty of Engineering, Hokkaido University, [3]Faculty of Information Science and Technology, Hokkaido University, Japan)

P10 BEOL-Compatible Microwave Annealing of HfO_2/ZrO_2 Superlattice Super High-K: Stabilizing Morphotropic Phase Boundaries and Low Leakage Current

Chen-You Wei[1], Yu-Hong Chen[2], Yi-Ju Yao[1], Guang-Li Luo[3], Fu-Ju Hou[3], Yung-Chun Wu[1,2] ([1]College of Semiconductor Research, [2]Department of Engineering and System Science, National Tsing Hua University, [3]Taiwan Semiconductor Research Institute, , Taiwan)

P11 Design Optimization of SiC CMOS FinFET for High-Temperature Next-generation SoC Logic Applications

Tae Seong Kwon[1,2], Young Jo Kim[1], Hyoung Woo Kim[1], Young Jun Yoon[3], Jae Hwa Seo[1], Sung Yun Woo[2] ([1]Advanced Semiconductor Research Center, Power Semiconductor Research Division, Korea Electrotechnology Research Institute (KERI), [2]School of Electronic and Electrical Engineering, Kyungpook National University, [3]School of Electronics and Mechanical Engineering, Gyeongkuk National University, Korea)

P12 XNOR Logic Implementation Using a Single Steep-Switching Positive Feedback Device

Jisung Im[1], Hansol Kim[1], Hojin Moon[1], Eunjeong Jang[1], Jong-Ho Bae[2], Sung Yun Woo[1] ([1]School of EE, Kyungpook National University, [2]School of SSE, Yonsei University, Korea)

P13 Reliability Characterizations on the Hybrid Hot-Cold Data Conversion in 3D NAND Flash Memory under Various Temperatures

Yujiao Ding[1], Ruidong Li[2], Yining Zhou[1], Xinghao Wang[1], Peng Guo[3], Yixuan Fan[1], Pengpeng Sang[1], Jixuan Wu[1], Xuepeng Zhan[1], Jiezhi Chen[1] ([1]Shandong Univ., China, [2]Cloud Computing Equipment Industry Innovation Co., Ltd., China, [3]Shandong Sinochip Semiconductors Co. Ltd., Jinan, China)

P14 Synaptic Emulated by Double-layer ZnO Resistive RAM (ReRAM) via Optimized Sputter and Low-temperature ALD Process

Xuepeng Zhan[1], Junyao Mei[1], Yuzhe Hu[1], Yifan Wu[1], Hongyang Zhang[1], Pengpeng Sang[1], Jixuan Wu[1], Jiezhi Chen[1] ([1] University, China, [2]Cloud Computing Equipment Industry Innovation Co., Ltd., Jinan, China, [3]Shandong Sinochip Semiconductors Co. Ltd, Jinan, China)

P15 Flash-based Computing-in-Memory (CiM) Architectures for High-accuracy Classification

Yixuan Fan[1], Yang Feng[1], Jixuan Wu[1], Jing Liu[2], Junyu Zhang[3], Zhi Liu[1], Xuepeng Zhan[1], Jiezhi Chen[1] ([1]Shandong University, China, [2]Key Laboratory of Microelectronic Devices and Integrated Technology, Institute of Microelectronics of Chinese Academy of Sciences, China, [3]Neumem Co., Ltd, Hefei, China)

P16 Learning with Fewer States: A Robust On-Chip Learning Algorithm Resilient to Conductance State Constraints in RRAM-based Neural Networks

Zhixing Cai[1], Jingwei Sun[1], Zongwei Wang[1], Zhizhen Yu[1], Ruiqing Xie[1], Zezhi Cheng[1], Lin Bao[1], Zheng Zhou[1], Ling Liang[1], Yimao Cai[1] ([1]School of Integrated Circuits, Peking University, China, [2]Beijing Advanced Innovation Center for Integrated Circuits, Peking University, China)

P17 Experimental Study on Double-layer ZnO Resistive RAM (ReRAM) by Co-optimized Sputtering and Low-temperature ALD Processes

Junyao Mei[1], Ruidong Li[2], Yifang Wu[1], Di Wu[1], Bo Chen[1], Peng Guo[3], Pengpeng Sang[1], Jixuan Wu[1], Xuepeng Zhan[1], Jiezhi Chen[1] ([1]Shandong University, China, [2]Cloud Computing Equipment Industry Innovation Co., Ltd., China, [3]Shandong Sinochip Semiconductors Co. Ltd., Jinan, China)

P18 Reliability Analysis of CFETs Under Various NBTI Conditions

Hsiang-Ting Kung[1], Narasimhulu Thoti[2], Hannu-Pekka Komsa[2], Ying-Tsan Tang[1] ([1]National Central University, Taiwan, [2]University of Oulu, Finland)

P19 A Ballistic Transport Model for Nanosheet CFETs with Si(100), (110), and (111) Channel Orientations

Yung-Chin Yang[1], Hung-Ming Tsai[1], Te-Kung Chiang[2], and Yeong-Her Wang[1]* ([1]National Cheng-Kung University, Taiwan, [2]National University of Kaohsiung, Taiwan)

P20 Quantitative Analysis of Endurance–dependent Charge Trapping Dynamics in Ferroelectric Field–Effect Transistors with Temperature Effects

Hyojin Yang[1], Haesung Kim[1], Changhyeon Han[3], Yoon Jung Lee[1], Sung-Jin Choi[1], Dae Hwan Kim[1], Dong Myong Kim[4], Daewoong Kwon[3], Jong-Ho Bae[2] ([1]Kookmin University, Korea, [2]Hanyang University, Korea, [3]DGIST, Korea, [4]Yonsei University, Korea)

P21 Analysis of Grain Boundary Effects Based on Location in a Diode-Type NAND Flash Memory Cell

Jinsu Kim[1], Hansol Kim[2], Hojin Moon[2], Wonjun Song[2], Jong-Ho Bae[3], Nagyong Choi[4], Sung Yun Woo[1,2] ([1]School of SCE, Kyungpook National University, Korea, [2]School of EEE, Kyungpook National University, Korea, [3]Dept. of SSE, Yonsei University, [4]Dept. of ECE, Seoul National University, Korea)

P22 Evaluation of In-Memory Logic Computation for Ferroelectric Capacitive Memory

Hao-Hsiang Chang[1], Po-Tsang Huang[1], Pin Su[1] ([1]Institute of Pioneer Semiconductor Innovation, [2]International College of Semiconductor Technology, [3]Institute of Electronics, National Yang Ming Chiao Tung University, Taiwan)

P23 Volatile and Nonvolatile Resistive Switching in Wafer-Scale MoS_2 Memristors

Yuan Fa[1,2], Dennis Braun[2], Lukas Völkel[2], Holger Lerch[1], Holger Kalisch[2], Michael Heuken[2,3], Andrei Vescan[2], Zhenxing Wang[1], Max C. Lemme[1,2] ([1]AMO GmbH, Advanced Microelectronic Center Aachen, Germany, [2]RWTH Aachen University, Germany, [3]AIXTRON SE, Germany)

P24 Impact of Oxygen Vacancies on Switching Behavior of Ferroelectric HfO2 from First Principle

Chenxi Yu[1], Xujin Song[1], Jiajia Zhang[1], Dijiang Sun[1], Xiaoyan Liu[1], Fei Liu[1], Jinfeng Kang[1] ([1]School of Integrated Circuits, Peking University, China)

P25 Tunable Tunnel Coupling in Vertically Stacked Symmetric FinFET-Based Ge Double Quantum Dots

Hua Yang[1], Wei-Yuan Lai[1], Ying-tsan Ethan Tang[1] ([1]National Central University, Taiwan)

P26 Numerical Investigation of Electrical Performance and Scaling Properties in 6T1C IGZO-Based Synaptic Devices

Ye-Han Kwon[1], Youngchae Roh[2], Changhoon Joe[2], Sangbum Kim[2], Sung-Min Hong[1] ([1]Gwangju Institute of Science and Technology, Korea, [2]Seoul National University, Korea)

P27 Investigation of Asymmetric Ferroelectric Switching in AlScN MFM Capacitors

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P28 Phosphorus Incorporation and Ionization in Ultra-Thin Silicon Films

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P29 All-in-one Monolithic 3D Heterostructured Integration of BEOL-Complementary N-Si FinFET / P-CNFET for Smart Edge Processing

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P30 Machine Learning-Driven Modeling for Fast and Accurate Z-Interference Estimation in 3D NAND Scaling

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P31 The Impacts of Different Producing Methods on the Memristive Performance in Monolayer CBRAM

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P32 Displacement Damage Effects Induced by Proton Irradiation in β-Ga2O3 Schottky Barrier Diodes

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P33 Determination of sensitivity limits for single molecule detection using single-electron sensing devices

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