

2025 Silicon Nanoelectronics Workshop 2025

June 8th-9th, 2025

Rihga Royal Hotel, Kyoto, Japan

Sunday, June 8th, 2025

8:30 Opening remarks

Kuniyuki Kakushima (Institute of Science Tokyo)

Session 1: Plenary Talks

Session Chair: Kuniyuki Kakushima (Institute of Science Tokyo)

8:40 1-01 (Plenary 1)

Amorphous Oxide Semiconductors for Memory Applications

Hideo Hosono (Institute of Science Tokyo & National Institute of Materials Science, Japan)

9:10 1-02 (Plenary 2)

Engineering High Quality Qubits in Silicon with Atomic Precision

Michelle Y. Simmons (Silicon Quantum Computing & University of New South Wales, Australia)

9:40-9:50 Break

Session 2: Stacked Architecture and 3D Integration

Session Chairs: Katsuhiko Tomioka (Hokkaido University) & Masaharu Kobayashi (The University of Tokyo)

9:50 2-01 (Oral 1)

First Realization of ALD based Sn-Doped InGaZnO with Reliability Enhancements for Monolithic 3D Integration

Sung-Hun Kim¹, Sun Hong Choi¹, Kota Sakai¹, Takuya Saraya¹, Toshiro Hiramoto¹, and Masaharu Kobayashi^{1,2} (¹Institute of Industrial Science, The University of Tokyo, ²d.lab, The University of Tokyo, Japan)

10:10 2-02 (Oral 2)

All-in-one Monolithic 3D Heterostructured Integration of BEOL- Complementary N-Si FinFET / P-CNFET for Smart Edge Processing

Shuang Liu^{1,2}, Feixiong Wang^{1,2}, Heyi Huang^{1,2}, Yadong Zhang^{1,2}, Yanqing Li^{1,2}, Yanzhao Wei^{1,2}, Huaxiang Yin^{1,2} (¹Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, ²School of Integrated Circuits, University of Chinese Academy of Sciences, Beijing, China)

10:30 2-03 (Oral 3)

Optimizing CFET Parasitic Capacitance and Performance Through Middle Dielectric Isolation and Middle Via Integration

Meng-Lin Wu¹, Yu-Cheng Lu², and Vita Pi-Ho Hu^{1,2} (¹Graduate Institute of Electronics Engineering, National Taiwan University, ²Graduate School of Advanced Technology, National Taiwan University, Taiwan)

10:50-11:00 Break

Session 3: Silicon Quantum Devices

Session Chairs: Takahide Oya (Yohokama National University) & Pei-Wen Li (National Yang Ming Chiao Tung University (NYCU))

11:00 3-01 (Invited 1)

Room Temperature Dopant-Atom Quantum Dot Transistors in Silicon

Zahid Durrani¹ (¹Imperial College London, UK)

11:25 3-02 (Oral 4)

Experimental Demonstration of Vertically Stacked Parallel Silicon Quantum Dots

Daiki Futagi¹, Junoh Kim¹, Tomoko Mizutani¹, Takuya Saraya¹, Hiroshi Oka², Takahiro Mori², Masaharu Kobayashi^{1,3}, Toshiro Hiramoto¹ (¹IIS, The Univ. of Tokyo, ²AIST, ³d.lab, The Univ. of Tokyo, Japan)

11:45 3-03 (Oral 5)

Parallel Silicon Single-Electron Pumps for Generating Nanoampere Current

Gento Yamahata¹, Takase Shimizu¹, Katsuhiko Nishiguchi¹, Akira Fujiwara¹ (¹NTT Basic Research Laboratories, Japan)

12:05 3-04 (Oral 6)

High-Temperature Single-Electron Tunneling Through P-donors Affected by Confinement

Pooja Sudha¹, Soumya Chakraborty¹, Daniel Moraru², Arup Samanta¹ (¹Indian Institute of Technology Roorkee (India), ²Research Institute of Electronics, Shizuoka University, Japan)

12:25-13:30 Lunch break

Session 4: Advanced Logic and Memory Devices

Session Chairs: Steve Chung (National Yang Ming Chiao Tung University (NYCU)) & Kasidit Toprasertpong (The University of Tokyo)

13:30 4-01 (Invited 2)

High-Performance BEOL-Compatible ALD-IGZO Top-Gate Radio-Frequency Transistors

Yanqing Wu¹, Shenwu Zhu¹, Qianlan Hu¹, Anyu Tong¹ (Peking University, China)

13:55 4-02 (Oral 7)

Vertical Channel Transistor-Based OS-Si Hybrid Gain Cell for High-Density and High-Retention Embedded DRAM

Yu-Hsuan Chuang¹, Vita Pi-Ho Hu¹ (¹National Taiwan University, Taiwan)

14:15 4-03 (Oral 8)

Below 10A CMOS-Double CFETs with Dielectric-wall-stress by Isolation-last Process for 0.0069 μm^2 of SRAM-cell Design

Yi-Sung Chen², Yu-Shang Shih², Hao-Ming Huang², Ting-Kuan Ma², E Ray Hsieh¹ (¹National Yang Ming Chiao Tung University, ²National Central University, Taiwan)

14:35 4-04 (Oral 9)

RRAM-Based In-Memory Stochastic Computing for Naïve Bayes Classifiers

Haoran Wang¹, Zongwei Wang¹, Yabo Qin, Lin Bao, Yimao Cai¹ (¹Peking Univ., China)

14:55-15:05 Break

Session 5: Memory and Related Technologies

Session Chairs: Minoru Oda (Kioxia) & Katsuhiko Nishiguchi (NTT Basic Research Laboratories)

15:05 5-01 (Oral 10)

Observation of State Change in 40nm TaOX ReRAM Cells during Read-disturb

Shota Suzuki¹, Naoko Misawa¹, Chihiro Matsui¹, and Ken Takeuchi¹

1Dept. of Electrical Engineering and Information Systems, The University of Tokyo, Japan

15:25 5-02 (Oral 11)

Performance Evaluation of 3D 1T-nC Ferroelectric RAM Architectures

Wei-Chen Chen¹, Hang-Ting Lue¹, Keh-Chung Wang¹, and Chih-Yuan Lu¹ (¹Macronix International Co., Ltd., Taiwan)

15:45 5-03 (Oral 12)

Thermally Stable Vertical-Stacked 1T1C FeRAM with Record 3.3 $\mu\text{F}/\text{cm}^2$ CMW Based on Unified Ferroelectric-Oxide Semiconductor Stack

Xujin Song^{1,2†}, Dijiang Sun^{1,2†}, Jiajia Zhang^{1,2}, Chenxi Yu^{1,2}, Xiaoyan Liu^{1,2}, Jinfeng Kang^{1,2*} (¹Peking University, ²Beijing Advanced Innovation Center for Integrated Circuits, China)

16:05 5-04 (Oral 13)

InAs/AlSb III-V NVM with High-speed (5ns) Low-power (1V) QW-tunnel Program for 10-year Storage by 2DEG-enhanced Retention

Jun Sheng Hou¹, Zi Yao Chung², Min Jie Chen², Ren Fu Ye¹, Li Cheng Chen¹, E Ray Hsieh^{3,*}, Jen-Inn Chyi¹ (¹National Central Univ., ²National Yang Ming Chiao Tung Univ., Taiwan)

16:25 5-05 (Oral 14)

A Novel Cross-Point Ferroelectric-Capacitor Array based Parallel In-Memory Encryption for Energy-Efficient Secure-AI Applications

Shengjie Cao¹, Weikai Xu¹, Zhiyuan Fu², Minyue Deng¹, Zebin Zhang¹, Qianqian Huang^{1,3*} and Ru Huang^{1,3*} (¹Peking University, China, ²Southeast University, China, ³Beijing Advanced Innovation Center for Integrated Circuits, China)

16:45-17:00 Break

Session 6: Poster session with shot-gun presentations

17:00-18:30 Starting with short oral presentations (17:00~17:35)

Session Chairs: Daniel Moraru (Shizuoka University) & Katsuhiko Nishiguchi (NTT Basic Research Laboratories)

(List of posters is available at the end.)

Monday, June 9th, 2025

Session 7: Advanced Electronics on New Materials

Session Chairs: Louis Hutin (CEA Leti) & Takahiro Shinada (Tohoku University)

8:30 7-01 (Invited 3)

Capacitor-less IGZO based gain cell (2T0C): A disruptive technology for high-density eDRAM and 3D-DRAM

Attilio Belmonte¹, Hyungrock Oh¹, Nouredine Rassoul¹, Subhali Subhechha¹, Adrian Chasin¹, Daisuke Matsubayashi¹, Yiqun Wan¹, Harold Dekkers¹, Romain Delhougne¹, Gouri Sankar Kar¹ (¹imec, Belgium)

8:55 7-02 (Oral 15)

BEOL-Compatible IGZTO Thin-Film Transistors with Ultra-High Positive Bias Stress Stability for Advanced Electronics

Kai Chen^{1,2}, Xiaonan Wu^{1,2}, Ran Cheng¹, Rui Zhang¹, Junkang Li^{1*}, Yunlong Li^{1,2*} (¹Zhejiang University, China, ²Zhejiang ICsprout Semiconductor Co., Ltd, China)

9:15 7-03 (Oral 16)

Enhanced Electrical Characteristics of Ge MOS Device by In-situ Low Temperature H₂ Treatment

Pai-Yu Hsiao^{1,†}, Dun-Bao Ruan^{2,†}, and Kuei-Shu Chang-Liao^{1*}, Hsin-I Yeh¹, Chih-Wei Liu¹, Yu-Hsuan Chien¹, Bo-Lien Kuo¹, Kai-Chun Yang¹, Cheng-Han Li¹, Cheng-Yu Wu¹ (¹National Tsing Hua University, Taiwan, ²Fuzhou University, China)

9:35 7-04 (Oral 17)

Synergistic Impact of Random Phase Distribution and Polarization Strength Variations on FeFET Across Grain Sizes and Ferroelectric Percentages

Yi-Ming Tseng^{1*} and Vita Pi-Ho Hu^{1,2**} (¹National Taiwan University, Taiwan, ²National Taiwan University, Taiwan)

9:55 7-04 (Oral 18)

Unified Memcapacitor-Memristor Memory for Synaptic Weights and Neuron Temporal Dynamics

S. D'Agostino^{1*}, M. Massarotto^{2*}, T. Torchet³, F. Moro³, N. Castellani¹, L. Grenouillet¹, Y. Beilliard¹, D. Esseni², M. Payvand³, and E. Vianello^{1†} (¹CEA, LETI, Universite Grenoble Alpes, France, ²DPIA, Universita degli Studi di Udine, Italy, ³University of Zurich and ETH Zurich, Switzerland)

10:15 7-05 (Oral 19)

Poly-Si Nanosheet FETs With Vertical C-Shaped Channel Using Pulse Laser Crystallization

Jinbiao Liu¹, Zhuo Chen¹, Yongkui Zhang¹, Junfeng Li¹, Xianglie Sun², Shujuan Mao², Guilei Wang², Chao Zhao², Huilong Zhu¹, and Jun Luo¹ (¹Institute of Microelectronics, Chinese Academy of Sciences, ²Beijing Superstring Academy of Memory, China)

10:35-10:45 Break

Session 8: Advanced CMOS Devices

Session Chairs: Hiroaki Satoh (Shizuoka Univ.) & Runsheng Wang (Peking University)

10:45 7-06 (Oral 20)

Heterojunction Tunneling and Reverse Shockley–Read–Hall Recombination Effects in Si_{1-x}Ge_x Channel/Si SDE CFETs for Steeper Subthreshold Swing and Low DIBL

Pei-lun Chang, Ying-Tsan Tang* (National Central University, Taiwan)

11:05 8-02 (Oral 21)

Statistical Analysis of Subthreshold Current Distributions in bulk MOSFETs at Room and Cryogenic Temperatures

Tomoko Mizutani¹, Kiyoshi Takeuchi¹, Takuya Saraya¹, Hiroshi Oka², Takahiro Mori², Masaharu Kobayashi¹, Toshiro Hiramoto¹ (¹Univ. of Tokyo, ²AIST, Japan)

11:25 8-03 (Oral 22)

Investigation on Enhanced Hot Carrier Degradation in FinFETs at Cryogenic Temperature

Zirui Wang¹, Zuoyuan Dong^{1,2}, Hongbo Wang¹, Zixuan Sun¹, Yue-Yang Liu³, Xing Wu², Runsheng Wang¹ (¹Peking Univ., ²East China Normal Univ., ³Inst. of Semiconductors, China)

11:45 8-04 (Oral 23)

Study of Current Inflections in Reverse Bias in Nano-dimensional Silicon Esaki Diodes

Daris Alfafa^{1,2}, Arief Udhiarto², Daniel Moraru^{1,3} (¹Graduate School of Sci. and Tech., Shizuoka Univ. (Japan), ²Department of Electrical Eng., Univ. of Indonesia (Indonesia), ³Res. Inst. of Electronics, Shizuoka Univ., Japan)

12:05 8-05 (Oral 24)

Deep Learning to Automate Fitting and Parameter Extraction of 2D Transistors

Robert K. A. Bennett¹, Harmon F. Gault¹, Asir Intisar Khan¹, Lauren Hoang¹, Tara Peña¹, Kathryn Neilson¹, Young Suh Song¹, Zhepeng Zhang², Andrew J. Mannix², Eric Pop^{1,2,3} (¹Stanford Univ., Dept. of Electrical Eng., ²Stanford Univ., Dept. of Materials Sci. & Eng., ³Stanford Univ., Dept. of Appl. Phys., USA)

12:25-13:30 Lunch break

Session 9: Interfaces and Reliability Engineering

Session Chairs: Michele Perego (CNR-IMM) & Toshifumi Irisawa (AIST)

13:30 9-01 (Invited 4)

Charge pumping electrically-detected magnetic resonance in Si MOS transistors — Identification of interface defects and dopant atoms —

Masahiro Hori (Research Institute of Electronics, Shizuoka University, Japan)

13:55 9-02 (Oral 25)

O/H Supercritical Fluid Passivation on Stacked Ge_{0.95}Si_{0.05} Nanosheet nFETs

Min-Kuan Lin¹, Ding-Wei Lin², Jui-Yu Hsu², Guan-Hua Chen², Bo-Hui Yu³, Wei-Jen Chen², Bo-Wei Huang², Tao Chou¹, Yi-Chun Liu², Yu-Rui Chen², Hong-Yi Tu⁴, Ting-Chang Chang⁵, and C. W. Liu^{1,2,3,*} (¹Graduate School of Advanced Technology, ²Graduate Institute of Electronics Engineering, ³Graduate Institute of Photonics and Optoelectronics, National Taiwan University, Taipei, Taiwan, ⁴Department of Materials and Optoelectronic Science, ⁵Department of Physics, National Sun Yat-Sen University, Kaohsiung, Taiwan)

14:15 9-03 (Oral 26)

Total Ionizing Doses Effects on MOSFET, FinFET, and GAAFET after Co-60 Radiation Exposure

Jing-Lin Zheng^{1,†}, Dun-Bao Ruan^{2,†}, and Kuei-Shu Chang-Liao^{1,*}, Shang-Hua Hsu¹ (¹National Tsing Hua University, Taiwan, ²Fuzhou University, China)

14:35 9-04 (Oral 27)

Improved Uniformity and Endurance of Ag-based Volatile Memristors via Annealing Engineering

Yading Yi^{1,3}, Xujin Song^{1,3}, Zhuohua Tang^{1,3}, Shangze Li^{1,3}, Dijiang Sun^{1,3}, Shiyue Song^{1,3}, Yulin Feng^{*2}, Zheng Zhou^{1,3}, Peng Huang^{1,3}, Jinfeng Kang^{1,3}, Lifeng Liu^{*1,3} (¹Peking University; ²Beijing Information Science and Technology University; ³Beijing Advanced Innovation Center for Integrated Circuits, China)

14:55-15:05 Break

Session 10: Quantum-Dot Devices

Session Chairs: Gento Yamahata (NTT Basic Research Laboratories) & Daniel Moraru (Shizuoka University)

15:05 10-01 (Invited 5)

Spatial Noise Correlation in Silicon Qubit Devices

Jun Yoneda¹ (¹Univ. of Tokyo (Japan))

15:30 10-02 (Oral 28)

Experimental Observation of Sequential Electron Incorporation within P-Donor Molecules in a Silicon Nano-Transistor

Soumya Chakraborty¹, Pooja Sudha¹, Hemant Arora¹, Daniel Moraru², Arup Samanta^{1,3} (¹Indian Institute of Technology Roorkee, India, ²Res. Inst. of Electronics, Shizuoka Univ., Japan, ³Centre of Nanotech., Indian Institute of Technology Roorkee, India)

15:50 10-03 (Oral 29)

Probing Low-Frequency Charge Noise in Few-Hole Physically-Defined Ge Quantum-Dot Single-Hole Transistors

Chi-Cheng Lai¹, Ting Tsai¹, Horng-Chih Lin¹, Pei-Wen Li¹ (¹National Yang Ming Chiao Tung University, Taiwan)

16:10 10-04 (Oral 30)

3D Stacked Silicon Quantum Dots Using Potential Barriers by Shared Gates

Junoh Kim¹, Daiki Futagi¹, Tomoko Mizutani¹, Takuya Saraya¹, Hiroshi Oka², Takahiro Mori², Masaharu Kobayashi^{1,3}, Toshiro Hiramoto¹ (¹IIS, The Univ. of Tokyo, ²AIST, ³d.lab, The Univ. of Tokyo, Japan)

16:30 10-05 (Oral 31)

Multiple-Electron Random Network System Simulation Based on Carbon Nanotube/Polyoxometalate Network

Shunya Watanabe¹, Takahide Oya¹ (¹Yokohama National University, Japan)

16:50-17:00 Break

Session 11: 30th Anniversary Panel Session

17:00-18:20 Silicon Nanoelectronics and Related Trends Over the Next 30 Years

Moderator: Daniel Moraru (Shizuoka University)

18:20-18:30 Closing Remarks (Daniel Moraru & SNW2026 Team)

List of Poster Presentations

P1 Integration of Optimized Superlattice $\text{HfO}_2/\text{ZrO}_2$ Dielectric into High-Performance Superlattice SiGe/Si p-type GAAFETs

Kai-Ting Huang¹, Yi-Ju Yao¹, Heng-Jia Chang², Chen-You Wei¹, Yu-Min Fu¹, Bo-Xu Chen², Tsai-Jung Lin¹, Yung-Teng Fang², Guang-Li Luo³, Fu-Ju Hou³, Yung-Chun Wu^{1,2} (¹College of Semiconductor Research, ²Department of Engineering and System Science, National Tsing Hua University, ³Taiwan Semiconductor Research Institute, Taiwan)

P2 BEOL-Compatible GAAFET Hybrid Memory Based on $\text{HfO}_2/\text{ZrO}_2$ Superlattice with Morphotropic Phase Boundary

Kuei-Chun Liao¹, Chen-You Wei¹, Yi-Ju Yao¹, Cheng-En Wu², Chien-Lung Chen², Chih-Chao Yang³, Guang-Li Luo³, Fu-Ju Hou³, Yung-Chun Wu^{1,2} (¹College of Semiconductor Research, ²Department of Engineering and System Science, National Tsing Hua University, ³Taiwan Semiconductor Research Institute, Taiwan)

P3 Study on the Application and Reliability of High-k $\text{HfO}_2/\text{ZrO}_2$ Superlattice Dielectrics in Ge Stacked Nanosheet GAAFET at 4K Ultra-Low Temperature

Kao Tsu-I¹, Huang Kai-Wei¹, Wei Chen-You², Lin Yi-Wen¹, Hou Fu-Ju³, Luo Guang-Li³, Wu Yung-Chun^{1,2} (¹Dept. of Engineering and System Science, ²College of Semiconductor Research, National Tsing Hua Univ., Taiwan, ³Taiwan Semiconductor Research Institute, Taiwan)

P4 Enhanced Reliability and Wake-Up Free Behavior of $\text{HfO}_2/\text{ZrO}_2$ Superlattice FeRAM With Triple-Level Cell Using High- and Low-Temperature ALD Stacks

Kuan-Wen Huang¹, Kun-Tao Lin¹, Yu-Yun Wang¹, Tien-Sheng Chao¹ (¹Department of Electrophysics, National Yang Ming Chiao Tung University, Taiwan)

P5 Implementation of Delay-Enabled Axons for Lightweight Neural Networks with Improving Accuracy in Edge Computing

GuangJin Li^{1,3}, Hao Ai^{1,3}, HaoKai Guan^{1,3}, LiHao Zhang^{1,3}, YuLin Feng², Zheng Zhou^{1,3}, Peng Huang^{1,3}, LiFeng Liu^{1,3} (¹School of Integrated Circuits, Peking University, China, ²Beijing Information Science and Technology University, China, ³Beijing Advanced Innovation Center for Integrated Circuits, China)

P6 Study of Single-Photon Detection Using a Back-Gated Si Single-Electron Transistor

Shogo Miyagawa¹, Jeygopi Panisilvam¹, Pooja Sudha², Arup Samanta², Daniel Moraru¹ (¹Research Institute of Electronics, Shizuoka Univ., Japan, ²Department of Physics, Indian Institute of Technology Roorkee, India, ³Centre of Nanotechnology, Indian Institute of Technology Roorkee, India)

P7 An Experimental Study on Hot-hole Injection (HHI) in Floating-gate (FG) Flash Memory

Chang Chen¹, Yang Feng¹, Jixuan Wu¹, Jing Liu², Junyu Zhang³, Xuepeng Zhan¹, Jiezhi Chen¹ (¹Shandong University, China, ²Institute of Microelectronics of Chinese Academy of Sciences, China, ³Neumem Co., Ltd, Hefei, China)

P8 BEOL-Compatible Annealing Effects on Properties of ALD NbO_x Films

Gaoqi Yang¹, Ruiqing Xie¹, Linbo Shan¹, Jiye Li¹, Zongwei Wang^{1,2}, Yimao Cai^{1,2} (¹School of Integrated Circuits, Peking University, China, ²Beijing Advanced Innovation Center for Integrated Circuits, Peking University, China)

P9 Multi-Level Split Weight Learning for Multi-Cell ReRAM Computation-in-Memory

Rei Kusunose¹, Seiji Adachi¹, Ayane Matsuzaki¹, Takao Marukame¹, Kota Ando¹, Tetsuya Asai¹ (¹Graduate School of Information Science and Technology, Hokkaido University, ²Faculty of Engineering, Hokkaido University, ³Faculty of Information Science and Technology, Hokkaido University, Japan)

P10 BEOL-Compatible Microwave Annealing of HfO₂/ZrO₂ Superlattice Super High-K: Stabilizing Morphotropic Phase Boundaries and Low Leakage Current

Chen-You Wei¹, Yu-Hong Chen², Yi-Ju Yao¹, Guang-Li Luo³, Fu-Ju Hou³, Yung-Chun Wu^{1,2} (¹College of Semiconductor Research, ²Department of Engineering and System Science, National Tsing Hua University, ³Taiwan Semiconductor Research Institute, , Taiwan)

P11 Design Optimization of SiC CMOS FinFET for High-Temperature Next-generation SoC Logic Applications

Tae Seong Kwon^{1,2}, Young Jo Kim¹, Hyoung Woo Kim¹, Young Jun Yoon³, Jae Hwa Seo¹, Sung Yun Woo² (¹Advanced Semiconductor Research Center, Power Semiconductor Research Division, Korea Electrotechnology Research Institute (KERI), ²School of Electronic and Electrical Engineering, Kyungpook National University, ³School of Electronics and Mechanical Engineering, Gyeongbuk National University, Korea)

P12 XNOR Logic Implementation Using a Single Steep-Switching Positive Feedback Device

Jisung Im¹, Hansol Kim¹, Hojin Moon¹, Eunjeong Jang¹, Jong-Ho Bae², Sung Yun Woo¹ (¹School of EE, Kyungpook National University, ²School of SSE, Yonsei University, Korea)

P13 Reliability Characterizations on the Hybrid Hot-Cold Data Conversion in 3D NAND Flash Memory under Various Temperatures

Yujiao Ding¹, Ruidong Li², Yining Zhou¹, Xinghao Wang¹, Peng Guo³, Yixuan Fan¹, Pengpeng Sang¹, Jixuan Wu¹, Xuepeng Zhan¹, Jiezhi Chen¹ (¹Shandong Univ., China, ²Cloud Computing Equipment Industry Innovation Co., Ltd., China, ³Shandong Sinochip Semiconductors Co. Ltd., Jinan, China)

P14 Synaptic Emulated by Double-layer ZnO Resistive RAM (ReRAM) via Optimized Sputter and Low-temperature ALD Process

Xuepeng Zhan¹, Junyao Mei¹, Yuzhe Hu¹, Yifan Wu¹, Hongyang Zhang¹, Pengpeng Sang¹, Jixuan Wu¹, Jiezhi Chen¹ (¹ University, China, ²Cloud Computing Equipment Industry Innovation Co., Ltd., Jinan, China, ³Shandong Sinochip Semiconductors Co. Ltd, Jinan, China)

P15 Flash-based Computing-in-Memory (CiM) Architectures for High-accuracy Classification

Yixuan Fan¹, Yang Feng¹, Jixuan Wu¹, Jing Liu², Junyu Zhang³, Zhi Liu¹, Xuepeng Zhan¹, Jiezhi Chen¹ (¹Shandong University, China, ²Key Laboratory of Microelectronic Devices and Integrated Technology, Institute of Microelectronics of Chinese Academy of Sciences, China, ³Neumem Co., Ltd, Hefei, China)

P16 Learning with Fewer States: A Robust On-Chip Learning Algorithm Resilient to Conductance State Constraints in RRAM-based Neural Networks

Zhixing Cai¹, Jingwei Sun¹, Zongwei Wang¹, Zhizhen Yu¹, Ruiqing Xie¹, Zezhi Cheng¹, Lin Bao¹, Zheng Zhou¹, Ling Liang¹, Yimao Cai¹ (¹School of Integrated Circuits, Peking University, China, ²Beijing Advanced Innovation Center for Integrated Circuits, Peking University, China)

P17 Experimental Study on Double-layer ZnO Resistive RAM (ReRAM) by Co-optimized Sputtering and Low-temperature ALD Processes

Junyao Mei¹, Ruidong Li², Yifang Wu¹, Di Wu¹, Bo Chen¹, Peng Guo³, Pengpeng Sang¹, Jixuan Wu¹, Xuepeng Zhan¹, Jiezhi Chen¹ (¹Shandong University, China, ²Cloud Computing Equipment Industry Innovation Co., Ltd., China, ³Shandong Sinochip Semiconductors Co. Ltd., Jinan, China)

P18 Reliability Analysis of CFETs Under Various NBTI Conditions

Hsiang-Ting Kung¹, Narasimhulu Thoti², Hannu-Pekka Komsa², Ying-Tsan Tang¹ (¹National Central University, Taiwan, ²University of Oulu, Finland)

P19 A Ballistic Transport Model for Nanosheet CFETs with Si(100), (110), and (111) Channel Orientations

Yung-Chin Yang¹, Hung-Ming Tsai¹, Te-Kung Chiang², and Yeong-Her Wang^{1*} (¹National Cheng-Kung University, Taiwan, ²National University of Kaohsiung, Taiwan)

P20 Quantitative Analysis of Endurance–dependent Charge Trapping Dynamics in Ferroelectric Field–Effect Transistors with Temperature Effects

Hyojin Yang¹, Haesung Kim¹, Changhyeon Han³, Yoon Jung Lee¹, Sung-Jin Choi¹, Dae Hwan Kim¹, Dong Myong Kim⁴, Daewoong Kwon³, Jong-Ho Bae² (¹Kookmin University, Korea, ²Hanyang University, Korea, ³DGIST, Korea, ⁴Yonsei University, Korea)

P21 Analysis of Grain Boundary Effects Based on Location in a Diode-Type NAND Flash Memory Cell

Jinsu Kim¹, Hansol Kim¹, Hojin Moon¹, Wonjun Song¹, Jong-Ho Bae², Nagyong Choi³, Sung Yun Woo¹ (¹School of SCE, Kyungpook National University, Korea, ²School of EEE, Kyungpook National University, Korea, ³Dept. of SSE, Yonsei University, ⁴Dept. of ECE, Seoul National University, Korea)

P22 Evaluation of In-Memory Logic Computation for Ferroelectric Capacitive Memory

Hao-Hsiang Chang¹, Po-Tsang Huang¹, Pin Su¹ (¹Institute of Pioneer Semiconductor Innovation, ²International College of Semiconductor Technology, ³Institute of Electronics, National Yang Ming Chiao Tung University, Taiwan)

P23 Volatile and Nonvolatile Resistive Switching in Wafer-Scale MoS₂ Memristors

Yuan Fa^{1,2}, Dennis Braun², Lukas Völkel², Holger Lerch¹, Holger Kalisch², Michael Heuken^{2,3}, Andrei Vescan², Zhenxing Wang¹, Max C. Lemme^{1,2} (¹AMO GmbH, Advanced Microelectronic Center Aachen, Germany, ²RWTH Aachen University, Germany, ³AIXTRON SE, Germany)

P24 Impact of Oxygen Vacancies on Switching Behavior of Ferroelectric HfO₂ from First Principle

Chenxi Yu¹, Xujin Song¹, Jiajia Zhang¹, Dijiang Sun¹, Xiaoyan Liu¹, Fei Liu¹, Jinfeng Kang¹ (¹School of Integrated Circuits, Peking University, China)

P25 Tunable Tunnel Coupling in Vertically Stacked Symmetric FinFET-Based Ge Double Quantum Dots

Hua Yang¹, Wei-Yuan Lai¹, Ying-tsan Ethan Tang¹ (¹National Central University, Taiwan)

P26 Numerical Investigation of Electrical Performance and Scaling Properties in 6T1C IGZO-Based Synaptic Devices

Ye-Han Kwon¹, Youngchae Roh², Changhoon Joe², Sangbum Kim², Sung-Min Hong¹ (¹Gwangju Institute of Science and Technology, Korea, ²Seoul National University, Korea)

P27 Investigation of Asymmetric Ferroelectric Switching in AlScN MFM Capacitors

Hirofumi Nishida¹, Si-Meng Chen¹, Takuya Hoshii¹, Kazuo Tsutsui¹, Hitoshi Wakabayashi¹, Kuniyuki Kakushima¹ (¹Institute of Science Tokyo, Japan)

P28 Phosphorus Incorporation and Ionization in Ultra-Thin Silicon Films

Andrea Pulici^{1,2}, Gabriele Seguini¹, Marco Fanciulli², Michele Perego¹ (¹CNR-IMM, Unit of Agrate Brianza, Italy, ²Università degli Studi di Milano-Bicocca, Italy)

P29 Controlling phosphorus doping at the nanoscale to promote synthetic spin orbit coupling in silicon

Michele Perego¹, Stefano Kuschlan¹, Francesc Perez-Murano², Jordi Llobet², Marta Fernandez-Regulez², Riccardo Chiarcos³, Michele Laus³, Gabriele Seguini¹, Andrea Pulici¹, Graziella Tallarida¹ (¹CNR-IMM, Unit of Agrate Brianza, Italy, ²Institute of

Microelectronics of Barcelona, Spain, ³Università del Piemonte Orientale “A. Avogadro”, Italy)

P30 Machine Learning-Driven Modeling for Fast and Accurate Z-Interference Estimation in 3D NAND Scaling

Hyeon Seo Yun¹, Jong Kyung Park¹ (¹Seoul National University of Science and Technology, Korea)

P31 The Impacts of Different Producing Methods on the Memristive Performance in Monolayer CBRAM

Xuepeng Zhan¹, Yuwei Qu¹, Hongyang Zhang¹, Yifan Wu¹, Di Wu¹, Bo Chen¹, Yixuan Fan¹, Pengpeng Sang¹, Jixuan Wu¹, Jiezhi Chen¹ (¹Shandong University, Qingdao, China, ²Cloud Computing Equipment Industry Innovation Co., Ltd., Jinan, China, ³Shandong Sinochip Semiconductors Co. Ltd, Jinan, China)

P32 Displacement Damage Effects Induced by Proton Irradiation in β -Ga₂O₃ Schottky Barrier Diodes

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P33 Determination of sensitivity limits for single molecule detection using single-electron sensing devices

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