2017 Silicon Nanoelectronics Workshop

June 4-5, 2017, Rihga Royal Hotel Kyoto, Kyoto, Japan

Call for Papers

Deadline for Abstracts: March 31, 2017

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General Information

The 2017 Silicon Nanoelectronics Workshop will be held at Rihga Royal Hotel Kyoto, Japan on June 4-5, 2016, just prior to VLSI Symposium on Technology as a satellite workshop of the VLSI Symposia. The workshop will focus on silicon-related nanoelectronics to bridge a gap between the Si nano-technology and the "real" VLSI world. The first Silicon Nanoelectronics Workshop was held in June, 1996 at Honolulu, Hawaii, USA. The 2017 Silicon Nanoelectronics Workshop will be the 22th in a series of annual workshops.

Scope

The workshop will cover various aspects of VLSI-related silicon nanoelectronics. Areas of interest include, but are not limited to:

- Sub-10 nm transistors employing conventional and novel architecture including non-classical structures, novel channel and source/drain materials, non-thermal injection mechanisms
- Device physics of nanodevices including quantum effects, nonequilibrium and ballistic transport
- Modeling and simulation of nanoscale devices
- Extreme processing of nanostructures, including nanopatterning
- Junction and insulator materials and process technology for nanodevices
- Nanoscale surface, interface, and heterojunction effects in nanodevices
- Device scaling issues including doping fluctuations and atomic granularity
- Novel architectures for nanodevices including quantum computing
- Optoelectronics using silicon nanostructures
- Devices for heterogeneous integration on silicon, including 2D materials, Ge and III-V, CNT, spin-based devices, MEMS and NEMS, etc.
- Environmental devices which contributes to low-carbon society (wireless sensors, energy harvesters, steep slope devices, etc.)

Submission of Abstract

Prospective authors are requested to submit a PDF file of the abstract ON-LINE at http://annex.jsap.or.jp/snw/

The abstract must consist of one page of text and one page of figures. The abstract must include the title, the author's names, affiliation, full address, phone and FAX numbers, and e-mail address. Faxed copies of the abstract will not be accepted. Accepted abstracts will be reproduced in the workbook exactly as received. The deadline for abstracts is **March 31, 2017**.
Questions may be addressed to **shinada@cies.tohoku.ac.jp** (T. Shinada)

Further Information

Registration forms and hotel reservation forms will be provided in the Web site of the 2017 VLSI Technology Symposium (http://www.vlsisymposium.org/). Some of the accepted papers will be presented in "Poster Sessions". Further information can be obtained at http://annex.jsap.or.jp/snw/