2017 Silicon Nanoelectronics Workshop

June 4 – 5, 2017
Rihga Royal Hotel Kyoto, Kyoto, Japan

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Sunday, June 4, 2017

8:30 **Opening remarks**
Kazuhiko Endo, *AIST*

Session 1: Plenary and tunnel devices

8:40 1-1 **[Plenary] Integrated III-V Nanoelectronic Devices on Si**
Heike Riel
IBM Research, Switzerland

9:10 1-2 **The Guideline on Designing Face-tunneling FET for Large-scale-device Applications in IoT**
E. R. Hsieh[1], J. W. Lee[2], M. H. Lee[2], and Steve S. Chung[1]
[1]Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, [2]Institute of Electro-Optical Science and Technology, National Taiwan Normal University

9:30 1-3 **Co-dopants induced Tunnel-Current Enhancement and Their Interaction in Silicon Nano Tunnel diode**
Manoharan Muruganathan[1], Daniel Moraru[2], Michiharu Tabe[2], Hiroshi Mizuta[1]
[1]School of Materials Science, Japan Advanced Institute of Science and Technology, [2]Research Institute of Electronics, Shizuoka University

9:50 1-4 **Negative Capacitance Tunnel FETs: Experimental Demonstration of Outstanding Simultaneous Boosting of On-current, Transconductance, Overdrive, and Swing**
A. Saeidi[1], F. Jazaeri[2], I. Stolichnov[1], G. V. Luong[3], Q. T. Zhao[3], S. Mantl[3], and Adrian M. Ionescu[1]
[1]Nanoelectronic Devices Laboratory, EPFL, [2]Integrated Circuits Laboratory, EPFL, [3]Peter Grünberg Institut 9 (PGI-9)

10:10 1-5 **A Study on W Vacancy Defect in Mono-layer Transition-Metal Dichalcogenide (TMD) TFETs through Systematic Ab initio Calculations**
Jixuan Wu[1, 2], Zhiqiang Fan[2], Jiezhi Chen[1], Xiangwei Jiang[2]
[1]School of Information Science and Engineering, Shandong University, [2]Institute of Semiconductors, Chinese Academy of Sciences

10:30 Break

Session 2: Modeling and characterization of advanced devices

10:50 2-1 **High Performance Ge pMOSFETs with Simultaneous Mobility ~412cm^2/V-s, EOT ~0.5 nm, I_{ON}/I_{OFF} ~10^5, Gate Leakage ~10^{-4} A/cm^2 by Modulating Interfacial Layer using Oxygen Deficient HfO_x**
Shih-Han Yi, Jiayi Huang, Chia-Wei Hsu, Tzung-Yu Wu, Dun-Bao Ruan and Kuei-Shu Chang-Liao
Department of Engineering and System Science, National Tsing Hua University

11:10 2-2 **Carrier-Separated Equivalent Circuit Modeling for Steep Subthreshold Slope PN-Body Tied SOI FET**
Daiki Ueda, Kiyoshi Takeuchi, Masaharu Kobayashi, and Toshiro Hiramoto
Institute of Industrial Science, The University of Tokyo

11:30 2-3 **Investigations on Dynamic Characteristics of Ferroelectric HfO_2 Based on Multi-Domain Interaction Model**
Kyungmin Jang, Nozomu Ueyama, Masaharu Kobayashi, and Toshiro Hiramoto
Institute of Industrial Science, The University of Tokyo

11:50 2-4 **Coincident Increment of Ferroelectricity and Leakage Current Emerged in Metal-Composition-Controlled Hf-Zr-O system**
Shinji Migita[1], Hiroyuki Ota[1], Hiroyuki Yamada[1], Akihito Sawa[1], and Akira Toriumi[2]
[1]AIST, [2]The University of Tokyo

12:10 2-5 **Uniformity Improvement of SiNx-based Resistive Switching Memory by Suppressed Internal Overshoot Current**
Min-Hwi Kim[1], Sungjun Kim[1], Suhyun Bang[1], Tae-Hyeon Kim[1], Dong Keun Lee[1], Seongjae Cho[2], Jong-Ho Lee[1], and Byung-Gook Park[1]
[1]Inter-University Semiconductor Research Center (ISRC) and the Department of Electrical and Computer Engineering, [2]Department of Electronic Engineering, Gachon University

12:30 Lunch

Session 3: Physics of atomistic devices

14:00 3-1 **[Invited] Ultimate Single Electronics with Silicon Nanowire MOSFETs**

Akira Fujiwara, Katsuhiko Nishiguchi, Gento Yamahata, and Kensaku Chida

NTT Basic Research Laboratories

14:30 3-2 **Electron Spin Relaxation of Single Phosphorus Donors and Donor Clusters in Atomically Engineered Silicon Devices**

Bent Weber[1,2], Yu-Ling Hsueh[2], Thomas F. Watson[1], Ruoyu Li,[4] Alexander R. Hamilton[4], Lloyd C. L. Hollenberg[5], Rajib Rahman[3], and Michelle Y. Simmons[2]

[1]Centre for Quantum Computation and Communication Technology, School of Physics, The University of New South Wales, [2]School of Physics & Astronomy, Monash University, [3]Network for Computational Nanotechnology, Purdue University, [4]School of Physics, The University of New South Wales, [5]Center for Quantum, Computation and Communication Technology, School of Physics, University of Melbourne

14:50 3-3 **Probing the Impact of Donor Quantum Dots with High-Bias Stability Diagrams in Selectively-Doped Si Nanoscale Transistors**

A. Afiff[1,3], A. Samanta[2], T. Hasan[1], A. Udhiarto[3], D. Hartanto[3], H. Sudibyo[3], M. Tabe[1] and D. Moraru[1]

[1]Research Institute of Electronics, Shizuoka University, [2]Indian Institute of Technology (IIT), [3]Faculty of Engineering, Universitas Indonesia

15:10 3-4 **Inter-band Tunneling Mechanisms via Dopant-induced Energy States**

G. Prabhudesai[1], G. Greeshma[1], M. Shibuya[1], M. Manoharan[2], H. Mizuta[2], M. Tabe[1], and D. Moraru[1]

[1]Research Institute of Electronics, Shizuoka University, [2]School of Materials Science, Japan Advanced Institute of Science and Technology

15:30 3-5 **Sensitive Detection of Holes Generated by Impact Ionization in Silicon**

H. Firdaus[1], M. Hori[1], Y. Takahashi[2], A. Fujiwara[3], Y. Ono[1]

[1]Research Institute of Electronics, Shizuoka University, [2]Graduate School of Information Science and Technology, Hokkaido University, [3]NTT Basic Research Laboratories

15:50 Break

Session 4: Variability and process control

16:00 4-1 **Suppressed Fin-LER Induced Variability in Negative Capacitance FinFETs**

Ho-Pei Lee and Pin Su

Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University

16:20 4-2 **Characteristics Variability of Gate-All-Around Polycrystalline Silicon Nanowire Transistors with Width of 10nm Scale**

Ki-Hyun Jang[1], Takuya Saraya[1], Masaharu Kobayashi[1], Naomi Sawamoto[2] and Atsushi Ogura[2], Toshiro Hiramoto[1]

[1]Institute of Industrial Science, The University of Tokyo, [2]School of Science and Technology, Meiji University

Session 5: Posters

16:50-18:30

16:50 Poster introductions (1 min each)

5-1 **Theoretical Analysis of Quasi-ballistic Hole Transport in Ge and Si Nanowires Focusing on Energy Relaxation Process**

Hajime Tanaka, Jun Suda, and Tsunenobu Kimoto

Department of Electronic Science and Engineering, Kyoto University

5-2 **Impacts of Diameter and Ge content Variation on the Performance of $Si_{1-x}Gex$ p-Channel Gate-All-Around Nanowire Transistors**

Xianle Zhang, Xiaoyan Liu, Longxiang Yin, Gang Du

Institute of Microelectronics, Peking University

5-3 I**mprovement of Dual-k spacer for Nanowire-FETs considering Circuit Delay and Electricstatic Controllability**

Hyungwoo Ko[1], Jongsu Kim[1], Dokyun Son[1], Myounggon Kang[2], and Hyungcheol Shin[1]

[1]Inter-university Semiconductor Research Center (ISRC) and School of Electrical Engineering and Computer Science, Seoul National University, [2]Department of Electronics Engineering, Korea National University of Transportation

5-4 **Analysis on Self Heating Effects in Nanowire FET Considering Effective Thermal Conductivity of BEOL**

Hyunsuk Kim[1], Dokyun Son[1], Ilho Myoung[1], Myounggon Kang[2], and Hyungcheol Shin[1]

[1]Department of Electrical Engineering and Computer Science, Seoul National University, [2]Department of Electronics Engineering, Korea National University of Transportation

5-5 **Analysis on Extension region in Nanowire FET Considering RC Delay and Electrical Characteristics**

Jongsu Kim[1], Changbeom Woo[1], and Myounggon Kang[2], and Hyungcheol Shin[1]

[1]Inter-university Semiconductor Research Center (ISRC) and Department of Electrical and Computer Engineering, Seoul National University, [2]Department of Electronics Engineering, Korea National University of Transportation

5-6 S**tudy on Random Telegraph Noise of Gate-All-Around Poly-Si Junctionless Nanowire Transistors**

Chen-Chen Yang, Kang-Ping Peng, Yung-Chen Chen, Horng-Chih Lin, and Pei-Wen Li

Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University

5-7 **Improved Electrical Characteristics and Reliability of Multi-Stacking PNPN Junctionless Transistors Using Channel Depletion Effect**

Ming-Huei Lin[1], Yi-Jia Shih[1], Chien Liu[2], Yu-Chien Chiu[1], Chia-Chi Fan[1], Guan-Lin Liou[3], Chun-Hu Cheng[3], and Chun-Yen Chang[1]

[1]Dept. of Electronics Engineering & [2]Dept. of Electro-physics, National Chiao Tung University, [3]Dept. of Mechatronic Engineering, National Taiwan Normal University

5-8 **A Novel Vertical Tunnel FET of Band-to-Band Tunneling Aligned with Gate Electric Field with Averaged SS of 28 mV/decade**

Pao-Chuan Shih[1], Hsien-Chih Huang[1], Chien-An Wang[2], and Jiun-Yun Li[1,2,3]

[1]Graduate Institute of Electronics Engineering, National Taiwan University, [2]Department of Electrical Engineering, National Taiwan University, [3]National Nano Device Laboratories

5-9 **Impact of Device Design Parameters on V_{DSAT} and Analog Performance of TFETs**

Abhishek Acharya, Sudeb Dasgupta and Bulusu Anand

Microelectronics and VLSI Group, Indian Institute of Technology Roorkee

5-10 **Dopant-Segregated Metal Source Tunnel Field-Effect Transistors with Schottky Barrier and Band-to-Band Tunneling**

Chun-Hsing Shih[1], Ting-Shiuan Kang[1,2], Yu-Hsuan Chen[1,2], Hung-Jin Teng[1], and Nguyen Dang Chien[3]

[1]Department of Electrical Engineering, National Chi Nan University, [2]Institute of Electronics Engineering, National Tsing Hua University, [3]Faculty of Physics, University of Dalat

5-11 **Fabrication of Nano-Wedge Resistive Switching Memory and Analysis on Its Switching Characteristics**

Dong Keun Lee, Sungjun Kim, Min-Hwi Kim, Suhyun Bang, Tae-Hyeon Kim, and Byung-Gook Park

Inter-university Semiconductor Research Center (ISRC) and Department of Electrical and Computer Engineering, Seoul National University

5-12 **Experimental Proof of Resonant Tunneling in MIIIS Devices Based on Ultra-Thin High-k Oxides and Intrinsic Quantum Well Formation**

Joel Molina Reyes[1], Hector Manuel Uribe Vargas[1]

[1]National Institute for Astrophysics, Optics and Electronics

5-13 **Possibility of Si Resonant Plasma-Wave Transistor as THz detector**

Jong Yul Park[1], and Sung-Ho Kim, and Kyung Rok Kim

[1]Electrical Engineering, Ulsan National Institute of Science and Technology

5-14 **Analysis of Metal gate Work-Function Variation for Vertical Nanoplate FET in 6-T SRAMs**

Kyul Ko[1], Dokyun Son[1], Myounggon Kang[2], and Hyungcheol Shin[1]

[1]Inter-university Semiconductor Research Center (ISRC) and Department of Electrical and Computer Engineering, Seoul National University, [2]Department of Electronics Engineering, Korea National University of Transportation

5-15 **Analysis of Parasitic Capacitance and Performance in Gate-All-Around and Tri-Gate Channel Vertical FET**

Youngsoo Seo[1], Myounggon Kang[2], and Hyungcheol Shin[1]

[1]Department of Electrical Engineering and Computer Science, Seoul National University, [2]Department of Electronics Engineering, Korea National University of Transportation

5-16 **Analysis of Self-Heating Effects in Vertical MOSFETs According to Device Geometry**

Ilho Myeong[1], Dokyun Son[1], Hyunsuk Kim[1], Myounggon Kang[2] and Hyungcheol Shin[1]

[1]Inter-university Semiconductor Research Center (ISRC) and Department of Electrical and Computer Engineering, Seoul National University, [2]Department of Electronics Engineering, Korea National University of Transportation

5-17 **In-depth analysis of self-heating effects in vertical nanoplate-shaped GAAFETs**

Dokyun Son[1], Ilho Myeong[1], Hyunsuk Kim[1], Myounggon Kang[2] and Hyungcheol Shin[1]

[1]Inter-university Semiconductor Research Center (ISRC) and Department of Electrical and Computer Engineering, Seoul National University, [2]Department of Electronics Engineering, Korea National University of Transportation

5-18 **Analysis of RC Delay for High Performance in LFET and VFET**

Changbeom Woo[1], Jongsu Kim[1], and Myounggon Kang[2], and Hyungcheol Shin[1]

[1]Inter-university Semiconductor Research Center (ISRC) and Department of Electrical and Computer Engineering, Seoul National University, [2]Department of Electronics Engineering, Korea National University of Transportation

5-19 **Gated-Thyristor DRAM Cell with Pillar Channel Structure**

Hyungjin Kim, Min-Woo Kwon, Myung-Hyun Baek, Sungmin Hwang, Sihyun Kim, Taejin Jang, Jeong-Jun Lee, Hyun-Min Kim, Kitae Lee, and Byung-Gook Park

Inter-University Semiconductor Research Center and Department of Electrical and Computer Engineering, Seoul National University

5-20 **Parameter Calibration of Drift-Diffusion Model in Quasi-Ballisitc Transport Region with Monte Carlo Method**

Lei Shen, Shaoyan Di, Longxiang Yin, Xiaoyan Liu and Gang Du

Institute of Microelectronics, Peking University

5-21 **Performance Assessment of a Graphene-Based Ballistic Switch Design**

Shamik Das and Nicolas S. Arango

Emerging Technologies Department, The MITRE Corporation

5-22 **A Boosted Common Source Line Program Scheme in Channel Stacked NAND Flash Memory with Layer Selection by Multilevel Operation**

Do-Bin Kim, Dae Woong Kwon, Seunghyun Kim, Sang-Ho Lee and Byung-Gook Park

Inter-university Semiconductor Research Center (ISRC) and the Department of Electrical and Computer Engineering, Seoul National University

5-23 **Effects of Nitride Trap Layer Properties on Location of Charge Centroid in Charge-Trap Flash Memory**

Seunghyun Kim[1], Do-Bin Kim[1], Eunseon Yu[2], Sang-Ho Lee[1], Seongjae Cho[2], and Byung-Gook Park[1]

[1]Inter-university Semiconductor Research Center (ISRC) and Department of Electrical and Computer Engineering, Seoul National University, [2]Department of Electronics Engineering, Gachon University

5-24 **Investigation on the RRAM Overshoot Current Suppression with Circuit Simulation**

Suyun Bang, Sungjun Kim, Min-Hwi Kim, Tae-Hyeon Kim, Dong Keun Lee, and Byung-Gook Park

Inter-university Semiconductor Research Center (ISRC) and Department of Electrical Engineering and ComputerEngineering, Seoul National University

5-25 **A New Operation Scheme to Obtain 3-bit Capacity per Cell in HfO_2 Based RRAM with High Uniformity**

Dongbin Zhu, Xiangxiang Ding, Peng Huang, Zheng Zhou, Xiaolu Ma, Lifeng Liu, Jinfeng Kang, Xing Zhang

Institute of Microelectronics, Peking University

5-26 **Evaluation of Multilevel Memory Capability of ReRAM Using Ta_2O_5 Insulator and Different Electrode Materials**

Yuanlin Li[1], Reon Katsumura[1], Mika Kristian Grö nroos[1], Atsushi Tsurumaki-Fukuchi[1], Masashi Arita[1], Hideyuki Andoh[2], Takashi Morie[2], and Yasuo Takahashi[1]

[1]Graduate School of Information Science and Technology, Hokkaido University, [2]Graduate School of Life Science and Systems Engineering, Kyushu Institute of Technology

5-27 **Characterization of Resistive Switching Memory Devices with Tunnel Barrier**

Sungjun Kim[1], Min-Hwi Kim[1], Tae-Hyeon Kim[1], Suhyun Bang[1], Dong keun Lee[1], Yao-Feng Chang[2], and Byung-Gook Park[1]

[1]Department of Electrical and Computer Engineering, Inter-University Semiconductor Research Center (ISRC), Seoul National University, [2]Microelectronics Research Center, The University of Texas at Austin

5-28 **Analysis of Two Divided Component of NBTI Framework using TCAD Simulation**

Shinkeun Kim[1], Youngsoo Seo[1], Dokyun Son[1], Myounggon Kang[2] and Hyungcheol Shin[1]

[1]Inter-university Semiconductor Research Center (ISRC) and Department of Electrical and Computer Engineering, Seoul National University, [2]Department of Electronics Engineering, Korea National University of Transportation

5-29 **Comparison of Parasitic Components between LFET and VFET using 3D TCAD**

Minsoo Kim[1], Hyungwoo Ko[1], Myounggon Kang[2] and Hyungcheol Shin[1]

[1]Inter-university Semiconductor Research Center (ISRC) and Department of Electrical and Computer Engineering, Seoul National University, [2]Department of Electronics Engineering, Korea National University of Transportation

5-30 **Simulation Study on Temperature Dependence of MOSFET and TFET-based pH-sensitive ISFET**

Sihyun Kim[1], Dae Woong Kwon[2], Ryoongbin Lee[1], Dae Hwan Kim[2], and Byung-Gook Park[1]

[1]Inter-University Semiconductor Research Center (ISRC) and Department of Electrical and Computer Engineering (ECE), Seoul National University, [2]Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, [3]School of Electrical Engineering, Kookmin University

5-33 **Undoped SiGe FETs With Metal-Insulator-Semiconductor Contacts**

Liang-Yu Chen, Yu-Feng Hsieh and Kuo-Hsing Kao

Department of Electrical Engineering of National Cheng Kung University

5-34 **GeSn N-FinFETs and NiGeSn Contact Formation by Phosphorus Implant**

Yen Chuang[1], Hsien-Chih Huang[1], and Jiun-Yun Li[1,2]

[1]Graduate Institute of Electronics Engineering, National Taiwan University, [2]National Nano Device Laboratories

5-35 **Atom Probe Study of Erbium and Oxygen Co-Implanted Silicon**

Yasuo Shimizu[1], Yuan Tu[1], Ayman Abdelghafar[2], Maasa Yano[2], Yudai Suzuki[2], Takashi Tanii[2], Takahiro Shinada[3], Enrico Prati[4], Michele Celebrano[5], Marco Finazzi[5], Lavinia Ghirardini[5], Koji Inoue , and Yasuyoshi Nagai[1]

[1]The Oarai Center, Institute for Materials Research, Tohoku University, [2]School of Science and Engineering, Waseda University, [3]Center for Innovative Integrated Electronic Systems, Tohoku University, [4]Istituto di Fotonica e Nanotecnologie, Consiglio Nazionale delle Ricerche, [5]Dipartimento di Fisica, Politecnico di Milano

5-36 **Program/Erase Speed and Data Retention Trade-Off in Negative Capacitance Versatile Memory**

Chia-Chi Fan[1], Yu-Chien Chiu[1], Chien Liu[2], Guan-Lin Liou[3], Wen-Wei Lai[1], Yi-Ru Chen[1], Tun-Jen Chang[1], Wan-Hsin Chen[2], Chun-Hu Cheng[3], and Chun-Yen Chang[1]

[1]Department of Electronics Engineering & [2]Department of Electro-physics, National Chiao-Tung University, [3]Department of Mechatronic Eng., National Taiwan Normal University

5-37 **Si-on-Insulator Grating Coupler Operating at 2 μm: Device Design, Fabrication, and Characterization**

Shengqiang Xu[1], Xin Guo[2], Yuan Dong[1], Wei Wang[1], Hong Wang[2], Xiao Gong[1], and Yee-Chia Yeo[1]

[1]Department of Electrical and Computer Engineering, National University of Singapore, [2]School of Electrical and Electronic Engineering, Nanyang Technological University

5-38 **Revisiting room-temperature 1.54 μm photoluminescence of ErOx centers in silicon at extremely low concentration**

Enrico Prati[1], Michele Celebrano[2], Lavinia Ghirardini[2], Paolo Biagioni[2], Marco Finazzi[2], Yasuo Shimizu[3], Yuan Tu[3], Koji Inoue[3], Yasuyoshi Nagai[3], Takahiro Shinada[4], Yuki Chiba[5], Ayman Abdelghafar[5], Maasa Yano[5], Takashi Tanii[5]

[1]Istituto di Fotonica e Nanotecnologie, Consiglio Nazionale delle Ricerche, [2]Dipartimento di Fisica, Politecnico di Milano, [3]Institute for Materials Research, Tohoku University, [4]Center for Innovative Integrated Electronic Systems, Tohoku University, [5]School of Science and Engineering, Waseda University

5-39 **Counter-intuitive Ge/Si/O interactions and Ge/Si symbiosis enable the creatation of new classes of exciting nanoelectronic and nanophotonic devices**

C. Y. Hsueh, T. L. Huang, K. P. Peng, M. H. Kuo, H. C. Lin, and Pei-Wen Li

Department of Electronic Engineering, National Chiao Tung University,

5-40 **Different Pixel Patterns of Si-Based Far Infrared Bolometers**

Feng-Renn Juang[1], Wen-Kuan Yeh[2], Wei-Chih Chen[1] and Ming-Feng Chung[1]

[1]Department of Electrical Engineering, National Sun Yat-sen University, [2]Department of Electrical Engineering, National University of Kaohsiung

5-41 **Graphene Heat Spreaders for Thermal Management of HBTs**

Wei-Min Tu, and Hsien-Cheng Tseng,

Department of Electronic Engineering, Kun Shan University

5-42 **Implementation of Inhibitory operation in Neuromorphic System**

Jeong-Jun Lee, Min-Woo Kwon, Hyungjin Kim, Sungmin Hwang, and Byung-Gook Park

Electrical and Computer engineering, Seoul National University

5-43 **Dual Gate Positive Feedback Field-Effect Transistor for Low Power Analog Circuit**

Min-Woo Kwon[1], Sungmin Hwang[1], Myung-Hyun Baek[1], Seongjae Cho [2], and Byung-Gook Park[1]

[1]Inter-university Semiconductor Research Center (ISRC) and Department of Electrical and Computer Engineering, Seoul National University, [2]Department of Electronic Engineering, Gachon University

5-44 **A 0.9-GHz Fully Integrated 45% PAE Class-E Power Amplifier Fabricated Using a 0.18-μm CMOS Process for LoRa Applications**

Yu-Ting Tseng[1] and Jeng-Rern Yang[2]

[1,2]Department of Communications Engineering, Yuan Ze University

5-45 **Ethanol Gas Sensor with Nanotree Arrays by Hydrothermal Method and Wet Etching**

Feng-Renn Juang and Chia-Pin Hsaio

Department of Electrical Engineering, National Sun Yat-sen University

Monday, June 5, 2017

Session 6: Plenary and 3D/heterogeneous integrations

8:30 6-1 **[Plenary] Harmonic innovatios in Semiconductor Devices and Computor Architectures toward Post "Moore-era"**
Yoshihiro Hayashi
The system device roadmap commiitte of Japan (SDRJ), Home & MCU Solutions Division, Renesas Electronics Corporation

9:00 6-2 **[Invited] More Moore: from device scaling to 3D integration and system-technology co-optimization**
Nadine Collaert
IMEC

9:30 6-3 **Positive Bias Temperature Instability of Tunnel Thin-Film Transistor for Applications of System-on-Panel and Three-Dimension Integrated Circuits**
William Cheng-Yu Ma, Hui-Shun Hsu, Che-Yu Jao, Chih-Cheng Fang and Tzu-Han Liao
Department of Electrical Engineering, National Sun Yat-sen University

9:50 6-4 **Very large photogain and high photorespone linearity of Ge-dot photoMOSFETs operating in accumulation-mode for monolithic Si photonics**
Ming-Hao Kuo[1], B. J. Liu[2], T. L. Huang[2], H. C. Lin[2], and Pei-Wen Li[1,2]
[1]Department of Electrical Engineering, National Central University, [2]Department of Electronic Engineering, National Chiao Tung University

10:10 Break

Session 7: 2D materials and devices

10:20 7-1 **[Invited] 2D Nanoelectronics: From Graphene to Silicene and Beyond**
Deji Akinwande
University of Texas at Austin

10:50 7-2 **Graphene-ZnO:N Schottky junction based thin film transistor**
S. Heo, Y.J. Kim, C.H. Kim, S.K. Lee, H.J. Lee, H.J.Hwang, J. Noh, and B.H. Lee
Center for Emerging Electronic Devices and Systems, School of Materials Science and Engineering, Gwangju Institute of Science and Technology

11:10 7-3 **Physisorption doping induced multiple dots behavior in graphene nanoconstrictions**

Takuya Iwasaki[1], Zhongwang Wang[1], Jamie Reynolds[2], Manoharan Muruganathan[1], and Hiroshi Mizuta[1]

[1]School of Materials Science, Japan Advanced Institute of Science and Technology, [2]Faculty of Physical Sciences and Engineering, Univ. of Southampton

11:30 7-4 **Fermi level modulation at the interface of graphene and metal**

Y.J. Kim, H.J. Lee, K.E.Chang, C.Cho, S.K.Lee and B.H. Lee

Center for Emerging Electric Devices and Systems, School of Material *Science and Engineering, Gwangju Institute of Science and Technology*

11:50 7-5 **Enhanced Asymmetry in Monolayer Graphene based Geometric Diodes**

Vikram Passi[1], Amit Gahoi[1], Max C. Lemme[1,2]

[1]University of Siegen, School of Science and Technology, [2]RWTH Aachen University

12:10 7-6 **BEOL compatible WS_2 transistors fully fabricated in a 300 mm pilot line**

T. Schram, Q. Smets, M.H. Heyne, B. Groven, E. Kunnen, A. Thiam, K. Devriendt, A. Delabie, D. Lin, D. Chiappe, I. Asselberghs, M. Lux, S. Brus, C. Huyghebaert, S. Sayan, A. Juncker*, M. Caymax, I.P. Radu

*IMEC, *COVENTOR*

12:30 Lunch

Session 8: Architectures for non-von Neumann computing

13:45 8-1 **[Invited] Harnessing Si CMOS Technology for Quantum Information**

L. Hutin[1], B. Bertrand[1], R. Maurand[2], M. Urdampilleta[3], B. Jadot[3], H. Bohuslavskyi[1,2], L. Bourdet[2], Y.-M. Niquet[2], X. Jehl[2], S. Barraud[1], C. Bäuerle[3], T. Meunier[3], M. Sanquer[2], S. De Franceschi[2], M. Vinet[1]

[1] CEA, LETI, [2]CEA INAC-PHELIQS, [3]Institut Néel

14:15 8-2 **28nm Fully-Depleted SOI Technology: Cryogenic Control Electronics for Quantum Computing**

H. Bohuslavskyi[1,2], S. Barraud[1], M. Cassé[1], V. Barral[1], B. Bertrand[1], L. Hutin[1], F. Arnaud[3], P. Galy[3], M. Sanquer[2], S. De Franceschi[2], and M. Vinet[1]

[1]CEA, LETI, [2]CEA, INAC-PHELIQS, [3]STMicroelectronics

14:35 8-3 **RRAM Based Convolutional Neural Networks for High Accuracy Pattern Recognition and Online Learning Tasks**
Z. Dong, Z. Zhou, Z.F. Li, C. Liu, Y.N. Jiang, P. Huang, L.F. Liu, X.Y. Liu, J.F. Kang
Institute of Microelectronics, Peking University

14:55 8-4 **RRAM-based Pattern Recognition System with Locally Inhibited Post-neurons**
Zheng Zhou, Peng Huang, Yuning Jiang, Zhe Chen, Chen Liu, Lifeng Liu, Xiaoyan Liu and Jinfeng Kang
Institute of Microelectronics, Peking University

15:15 8-5 **Investigation on the V_{dd} Scaling Limit of Stochastic Computing Circuits based on FinFET Technology**
Xiaobo Jiang, Runsheng Wang, Shaofeng Guo, Ru Huang
Institute of Microelectronics, Peking University

15:35 8-6 **Design of Majority Logic Gate for Single-Dopant Device**
Takahide Oya[1] and Takahiro Shinada[2]
[1]Graduate School of Engineering, Yokohama National University, [2]Center for Innovative Integrated Electronics System, Tohoku University

15:55 Break

Session 9: Panel Session

16:10-17:40

Topics: **Reinvent silicon device for next generation computing**
Moderator: Masaharu Kobayashi, *University of Tokyo*
Panelists: Nadine Collaert, *IMEC*
Deji Akinwande, *University of Texas at Austin*
Akira Fujiwara, *NTT Basic Research Laboratories*
Louis Hutin, *LETI*
Heike Riel, *IBM Zurich*

17:40 **Closing remarks**