2015 Silicon Nanoelectronics Workshop

June 14-15, 2015
Rihga Royal Hotel Kyoto, Kyoto, Japan

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Sunday, June 14, 2015

8:30 Opening Remarks
Yasuo Takahashi, Hokkaido University

Session 1: Plenary and Nonvolatile Memories

Session Co-Chairs: Kazuhiko Endo, AIST and Takahiro Shinada, Tohoku University

8:40 1-1 **(Plenary)** Advanced process technologies of 1S1R for High Density Cross Point ReRAM, B. Y. Kim and H. S. Kim (SK Hynix Inc.)

9:10 1-2 Trade-off of Performance, Reliability and Cost of SCM/NAND Flash Hybrid SSD, H. H. Takishita, S. Ning, and K. Takeuchi (Chuo University)

9:30 1-3 Additional Charge Trapping Layer SONOS Nonvolatile Memory Based on Ultra-Thin Body Poly-Si Junctionless FinFET, Wei-Cheng Wang, Chien-Chih Chung, Ming-Hsien Chung, Cheng-Ping Wang, Yung-Chun Wu (National Tsing Hua University)

9:50 1-4 Understanding the Underlying Physics of Superior Endurance in Bi-layered TaO_X-RRAM, Y. D. Zhao, P. Huang, Z. Chen, C. Liu, H. T. Li, W. J. Ma, B. Gao, X. Y. Liu, J. F. Kang (Peking University)

10:10 Break

Session 2: Novel Process Technology for Nanoelectronics

Session Co-Chairs: Kensuke Ota, Toshiba and Toshifumi Irisawa (AIST)

10:30 2-1 Variability Suppression of FinFETs by Smoothing Sidewall Roughness Using Ion Beam Etching Technology, T. Matsukawa[1], K. Endo[1], H. Akasaka[2], Y. Kamiya[2], M. Ikeda[2], K. Tsunekawa[2], T. Nakagawa[2], Y.X. Liu[1], and M. Masahara[1] ([1]AIST, [2]Canon ANELVA)

10:50 2-2 sSOI Relaxation by BOX Creep Technique for Dual Strain CMOS Integration, A. Bonnevialle[1,2], C. Le Royer[2], Y. Morand[1], S. Reboh[2], D. Rouchon[2], N. Bernier[2], B. Mathieu[2], C. Plantier[2], M. Vinet[2] ([1]STMicroelectronics, [2]CEA LETI)

11:10 2-3 Significance of Kinetic-linkage of Oxygen Vacancy with SiO_2/Si Interface for SiO_2-IL Scavenging in HfO_2 Gate Stacks, X. Li, T. Yajima, T. Nishimura, and A. Toriumi (The University of Tokyo)

11:30 2-4 Gate-stack engineering for self-aligned Ge-gate/SiO_2/SiGe-channel Insta-MOS devices, Wei-Ting Lai[1,2], Kuo-Ching Yang[2], Po-Hsiang Liao[2], Thomas George[2], and Pei-Wen Li[1,2] ([1]National Chiao Tung University, [2]National Central University)

11:50 2-5 Impact of H_2, O_2, and N_2 anneals on atomic-scale surface flattening for 3-D Ge channel architecture, Y. Morita, H. Ota, M. Masahara, and T. Maeda (AIST)

12:10 Lunch

Session 3: Nanowire FETs

Session Co-Chairs: Kristin De Mayer, IMEC and Hiroshi Mizuta, JAIST, University of Southampton

13:30 3-1 **(Invited)** Experimental Study of Reliabilities in Tri-gate Nanowire Transistor ~What is Main Reliability Issue in 3D Transistor?~, K. Ota, C. Tanaka, D. Matsushita, T. Numata, and M. Saitoh (Toshiba Corporation)

14:00 3-2 Threshold Voltage and Current Variability of Extremely Narrow Silicon Nanowire MOSFETs with Width down to 2nm, T. Mizutani, Y. Tanahashi, R. Suzuki, T. Saraya, M. Kobayashi, and T. Hiramoto (University of Tokyo)

14:20 3-3 Performance of GAA Poly-Si Channel of Junctionless Field Effect Transistors with Ultra-Thin Body, Yan-Bo Liu, Yi-Ruei Jhan, Cheng-Ping Wang, and Yung-Chun Wu (National Tsing Hua University)

14:40 3-4 Investigation of Reconfigurable Silicon Nanowire Schottky Barrier Transistors-Based Logic Gate Circuits and SRAM Cell, J. Wang, G. Du, and X. Y. Liu (Peking University)

15:00 3-5 Impacts of Surface Roughness Scattering on Hole Mobility in Germanium Nanowires, H. Tanaka, J. Suda, and T. Kimoto (Kyoto University)

15:20 Break

Session 4: Finite Dopants in Nanodevices

Session Chair: Steve S. Chung, National Chiao Tung University

15:35 4-1 **(Invited)** Single ion implantation of Ge donor impurity in silicon transistors, E. Prati [1], Y. Chiba[2], M. Yano[2], K. Kumagai[2], M. Hori[3], G. Ferrari[4], T. Shinada[5], and T. Tanii[2], [1]Consiglio Nazionale delle Ricerche, [2]Waseda University, [3]University of Toyama, [4]Politecnico di Milano, [5]Tohoku University)

16:05 4-2 Impact of Diffused Donor-Clusters near Lead/Channel Boundary on High-Temperature Single-Electron Tunneling in Narrow SOI-FETs, D. Moraru, A. Samanta[1], Y. Takasu[1], K. Tyszka[1,2], T. Mizuno[1], R. Jablonski[2] and M. Tabe[1] ([1]Shizuoka University, [2]Warsaw University of Technology)

16:25 4-3 The impact of single donor and donor-acceptor pair on electronic and transport properties of silicon nanostructures, L. T. Anh[1], D. Moraru[2], M. Manoharan[1], M.Tabe[2], and H. Mizuta[1,3] ([1]JAIST, [2]Shizuoka University, [3]Southampton University)

Session 5 Posters

16:45-18:30 Starting with Short Oral Presentation

Session Chairs: Mitsuru Takenaka, University of Tokyo and Kazuhiko Endo, AIST

5-1 Investigation of the Impact of Grain Boundary on Threshold Voltage of 3-D MLC NAND Flash Memory, Z. Lun, L. Shen, Y. Cong, G. Du, X. Liu, Y, Wang (Peking University)

5-2 Resistive Switching Characteristics in HfOx Memory Devices with Local Electrical Field Design, Tsung-Kuei Kang, Wei-Len Chen, Yu-Han Chen, Pei-Hsun Tsai (Feng-Chia University)

5-3 Position and Number Control of Donor-QD Potential by Pattern-doping in SOI-FET Channels, K. Tyszka[1,2], D. Moraru[1], T. Mizuno[1], R. Jablonski[2], M. Tabe[1] (Shizuoka University, Warsaw University)

5-4 Nanodamascene metal-insulator-metal single electron transistor prepared by atomic layer deposition of tunnel barrier and subsequent reduction of metal surface oxide, G. Karbasian, A. O. Orlov, and G. L. Snider (University of Notre Dame)

5-5 Impacts of Channel Constriction Dimensions of Graphene Single Carrier Transistors on the Coulomb Diamond Characteristics, T. Iwasaki[1], M. Muruganathan[1], and H. Mizuta[1,2], ([1]JAIST, [2]University of Southampton)

5-6 Series-triple quantum dots fabricated under each control gate by the use of thermal oxidation, T. Uchida[1], H. Sato[1], A. Tsurumaki-Fukuchi[1], M. Arita[1], A. Fujiwara[2], and Y. Takahashi[1] ([1]Hokkaido University, [2]NTT Corporation)

5-7 Fabrication and characterization of physically-defined double quantum dots without unintentional localized states on highly-doped silicon substrate, Y. Yamaoka, T. Kodera, S. Oda (Tokyo Institute of Technology)

5-8 Characterization of carrier dynamics in Ge quantum dots through Ge quantum-dot MOSFETs using pulsed voltage technique, Ming-Hao Kuo[1], Ho-Chane Chen[1], Wei-Ting Lai[1,2], and Pei-Wen Li[1,2] ([1]National Central University, [2]National Chiao Tung University)

5-9 Simultaneous two gate reflectometric spectroscopy of Si coupled donor-dot system, X. Jehl[1], A. O. Orlov[2], R. Maurand[1], P. Fay[2], G. L. Snider[2], S. Barraud[3], and M. Sanquer[1] ([1]DSM-INAC, [2]University of Notre Dame, [3]DRT-Leti)

5-10 Fabrication of a highly controllable Si-MOS quantum dot device, T. Honda[1], J. Yoneda[2,3], K, Takeda[2,3], T. Kodera[1,2], S. Tarucha[2,3], and S. Oda[1] ([1]Tokyo Institute of Technology, [2]The University of Tokyo, [3]RIKEN

5-11 Tunneling Field-Effect Transistor with a Grown Si Epitaxial Layer for Boosting ON Current, J. Lee, J. H. Kim, D. W. Kwon, E. Park, T. Hyung Park, and B.-G. Park (Seoul National University)

5-12 Short-Drain Effect of 5 nm Tunnel Field-Effect Transistors, Yu-Hsuan Chen[1], Nguyen Dang Chien[2], Jr-Jie Tsai[1], Yan-Xiang Luo[3], and Chun-Hsing Shih[1] ([1]National Chi Nan University, [2]University of Da Lat, [3]National Tsing Hua University)

5-13 Fabrication and Characterization of Silicon Nanowire Ultra-thin Channel Poly-Si Junctionless Field Effect Transistors with a Trench Structure Ko-Wei Lin, Mu-Shih Yeh, Min-Hsin Wu, Yung-Chun Wu (National Tsing Hua University)

5-14 Hybrid Channel Poly-Si Junctionless Field-Effect Transistors with Trench Structure Formed by Dry Etching Process, C.-P. Wang, Y.-R. Jhan, J.-J. Su, Y.-C. Wu (National Tsing Hua University)

5-15 Built-in Effective Body-Bias Effect in UTBB Hetero-Channel MOSFETs and Its Suppression, C.-H. Yu, P. Su (National Chiao Tung University)

5-16 Boolean logic circuit implementation using multi-input floating-body MOSFET, Min-Woo Kwon, Hyungjin Kim, Jungjin Park, Byung-Gook Park (Seoul National University)

5-17 Comparison of Electrical Characteristics of N-type Silicon Junctionless Transistors with and without Film Profile Engineering by TCAD Simulation, Jung-Ruey Tsai[1], Horng-Chih Lin[2], Hsiu-Fu Chang[1], Bo-Shiuan Shie[2], Ting-Ting Wen[2], and Tiao-Yuan Huang[2] (Asia University, National Chiao Tung University)

5-18 Thermodynamic stability of high phosphorus concentration in silicon nanostructures, M. Perego[1], G. Seguini[1], E. Arduca[1,2], J. Frascaroli[1], D. De Salvador[1,2], M. Mastromatteo[1,2], A. Carnera[1,2], G. Nicotra[1], M. Scuderi[1], C. Spinella[1], G. Impellizzeri[1], C. Lenardi[2], and E. Napolitani[1,2] ([1]IMM-CNR, [2]Università degli Studi di Padova)

5-19 3D-TCAD Simulation Study of the Novel T-FinFET Structure for Sub-14nm Metal-Oxide-Semiconductor Field-Effect Transistor, Chen-Han Chou, Chung-Chun Hsu, Steve S. Chung, Chao-Hsin Chien (National Chiao Tung University)

5-20 Characteristics of Inversion, Accumulation and Junctionless mode Silicon N-Type and P-Type Bulk FinFETs with optimized 3-nm nano-fin structure, V. Thirunavukkarasu, Y.-R. Jhan, Y.-B. Liu, and Y.-C. Wu (National Tsing Hua University)

5-21 Bringing Physics to Device Design - a Fast and Predictive Device Simulation Framework, M. Karner, Z. Stanojevic, F. Mitterbauer, C. Kernstock, H. Demel (Global TCAD Solutions GmbH)

5-22 A Capacitance-Voltage model for DG-TFET, A. Biswas, A. M. Ionescu (Ecole Polytechnique Fédérale de Lausanne)

5-23 Physics-based Model for the Conductive Filament at the Low Resistance State of Thin SiO_2 Films, R. Yamaguchi, S. Sato, and Y. Omura (Kansai University)

5-24 Performance Evaluation of Si Ultra-Thin Body (1 nm) Junctionless FET with L_G = 1 nm and L_G = 3 nm, Yi-Ruei Jhan, Yan-Bo Liu, Yung-Chun Wu (National Tsing Hua University)

5-25 Design and analysis of electric-field-assisted nonlocal silicon-channel spin devices, D.Kitagata, T.Akushichi, Y.Takamura, Y.Shuto, S.Sugahara (Tokyo Institute of Technology)

5-26 Silicon-Compatible Resonant Plasma-Wave Transistor with 2D Silicene Channel for High-Performance Terahertz Electromagnetic Wave Emitters, Jong Yul Park, Sung-Ho Kim, and Kyung Rok Kim (Ulsan National Institute of Science and Technology)

5-27 Novel Trigate Field-Plated Poly-Si TFT with Improved Leakage Current and High On/Off Current Ratio, Yong-Hong Syu, Hsin-Hui Hu*, Jhen-Yu Tsai, Kai-Ming Wang, Jia-Jin Tsa (National Taipei University of Technology)

5-28 Frequency-Dependent Response of Nanoscale Thermocouples Using Temperature Oscillations Produced by Nanoscale Heaters, Gergo P. Szakmany, Alexei O. Orlov, Gary H. Bernstein, Wolfgang Porod (University of Notre Dame)

Monday, June 15, 2015

Session 6: New Low-Power Devices

Session Co-Chairs: Byung-Gook Park, Seoul National University
and Enrico Prati,Consiglio Nazionale delle Ricerche

8:30 6-1 New features in Planar SiGe Channel Tunnel FETs Performance and Operation, C. Le Royer[1], L. Hutin[1], S. Martinie[1], P. Nguyen[1], S. Barraud[1], F. Glowacki[1], S. Cristoloveanu[2], M. Vinet[1] ([1]CEA LETI, [2]IMEP-LAHC)

8:50 6-2 Design of Complementary Tilt-gate TFETs with SiGe/Si and III-V Integrations Feasible for Ultra-low-power Applications E. R. Hsieh[1], Y. S. Lin[2], Y. B. Zhao[1], C. H. Liu[2], C. H. Chien[1], and Steve S. Chung[1] ([1]National Chiao Tung University, [2]National Taiwan Normal University)

9:10 6-3 Dopant-Assisted Tunnel-Current Enhancement in Two-Dimensional Esaki Diodes, H.N. Tan[1], D. Moraru1, K. Tyszka[1,2], A. Sapteka[3], S. Purwiyanti[3], L.T. Anh[4], M. Manoharan[4], T. Mizuno[1], R. Jablonski[2], D. Hartanto[3], H. Mizuta[4,5], M. Tabe[1] ([1]Sizuoka University, [2]Warsaw University of Technology, [3]University of Indonesia, [4]JAIST, [5]University of Southampton)

9:30 6-4 Fabrication of high-quality $Co_2FeSi_{0.5}Al_{0.5}$/CoFe/MgO/Si spin injectors for Si-channel spin devices, T. Kondo, Y. Kawame, Y. Takamura, Y. Shuto, S. Sugahara. (Tokyo Institute of Technology)

9:50 Break

Session 7: Quantum Computing and Electronics

Session Co-Chairs: Michiharu Tabe, Sizuoka University and Pei-Wen Li, National Central University

10:10 7-1 **(Invited)** Spin-based Quantum Computing in Silicon, A. Dzurak (UNSW)

10:40 7-2 Variation of Coulomb diamonds and excited states caused by electric field in Si single-electron transistor, H. Satoh[1], T. Uchida[1], A. Tsurumaki-Fukuchi[1], M. Arita[1], A. Fujiwara[2], and Y. Takahashi[1] ([1]Hokkaido University, [2]NTT Corporation)

11:00 7-3 Study of charged island formation in nanoscale Si single-electron transistors using dual port reflectometric spectroscopy, A. O. Orlov[1], P. Fay[1], G. L. Snider[1], X. Jehl[2], R. Lavieville[3], S. Barraud[3], and M. Sanquer[2] ([1]University of Notre Dame, [2]DSM-INAC, [3]DRT-Leti)

11:20 7-4 Low Temperature Charge Pumping in SOI Gated PIN Diode, T. Watanabe[1], M. Hori[1], T. Saruwatari[1], A. Fujiwara[2], and Y. Ono[1] ([1]University of Toyama, [2]NTT)

11:40 7-5 Charge sensing of p-channel double quantum dots fabricated on (110) silicon substrate, K. Iwasaki, T. Kodera, and S. Oda (Tokyo Institute of Technology)

12:00 Lunch

Session 8: Post Silicon Materials and Devices

Session Co-Chairs: Yukinori Ono, University of Toyama and Kazuhiko Endo, AIST

13:30 8-1 **(Invited)** Fluctuations and Relaxation in Graphene, D. K. Ferry, B. Liu, and R. Akis (Arizona State University)

14:00 8-2 Low pull-in voltage graphene nanoelectromechanical switches, M. Manoharan[1], T. Chikuba[1], N. Kanetake[1], J. Sun[1], and H. Mizuta[1,2] ([1]JAIST, [2]University of Southampton)

14:20 8-3 Challenges of 3D VLSI-CoolCube™ process with p-Ge-OI and n-InGaAs-OI for Ultimate CMOS Nodes, F. Nemouchi[1], L. Hutin[1], H. Boutry[1], P. Rodriguez[1], E. Ghegin[1,2], J. Borrel[1,2], Y. Morand[2], S. Kerdiles[1], P. Batude[1], and M. Vinet[1] (CEA Leti, STMicroelectronics)

14:40 8-4 CMOS Roadmap Analysis from the Perspective of III-V technology using MASTAR, G. Hiblot[1,2], Q. Rafhay[2], G. Mugny[1], G. Ghibaudo[2], and F. Boeuf[1] ([1]STMicroelectronics, [2]IMEP-LAHC)

15:00 8-5 Effect of Free Carrier Accumulation or Depletion on Zone-center Vibrational Mode in Ge, S. Kabuyanagi, T. Nishimura, T. Yajima, and A. Toriumi (The University of Tokyo)

15:20 8-6 N+/P Shallow Junction with High Dopant Activation and Low Contact Resistivity Fabricated by Solid Phase Epitaxy Method for Ge Technology, P. Liu, M. Li, X. An, M. Lin, Y. Zhao, B. Zhang, X. Xia, R. Huang (Peking University)

15:40 Break

Session 9: 20th Anniversary Panel Session

16:00-17:30

Moderator: T. Irisawa, AIST

Topics: Past and future of Si-nano related electronics

Panelists: D. Ferry (Arizona State University)
H. Iwai (Tokyo Institute of Technology)
S. Oda (Tokyo Institute of Technology)
T. Hiramoto (The University of Tokyo)
K. De Meyer (imec)

17:30 Closing Remarks