2019 Silicon Nanoelectronics Workshop

June 9 – 10, 2019
Rihga Royal Hotel Kyoto, Kyoto, Japan

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10:40 Break

Session 3: Neural Systems, New Computing and Modeling

Session Chair: Takahide Oya, *Yokohama National University*

11:00 3-1 **[Invited] Temporal feature analysis in brain-inspired neural systems**

Tomoki Fukai[1,2] and Toshitake Asabuki[3]

[1]Okinawa Institute of Science and Technology, [2]RIKEN, [3]The University of Tokyo

11:30 3-2 **An Improved Hardware Acceleration Architecture of Binary Neural Network with 1T1R Array Based Forward/Backward Propagation Module**

Yizhou Zhang, Zheng Zhou, Peng Huang, Mengqi Fan, Runze Han, Wensheng Shen, Lifeng Liu, Xiaoyan Liu, Jinfeng Kang

Peking University

11:50 3-3 **A Parallel Bitstream Generator for Stochastic Computing**

Yawen Zhang, Runsheng Wang, Xinyue Zhang, Zherui Zhang, Jiahao Song, Zuodong Zhang, Yuan Wang, Ru Huang

Peking University

12:10 3-4 **New-Generation Design-Technology Co-Optimization (DTCO): Machine-Learning Assisted Modeling Framework**

Zhe Zhang[1], Runsheng Wang[1], Cheng Chen[1], Qianqian Huang[1], Yangyuan Wang[1], Cheng Hu[2], Dehuang Wu[2], Joddy Wang[2], Yangyuan Wang[1]

[1]Peking University, [2]Synopsys

12:30 Lunch

Session 4: Energy Efficient Electronics and Memory

Session Chair: Steve Chung, *National Chiao Tung University*

14:00 4-1 **[Invited] Energy Efficient Nanoelectronics**

An Chen

IBM Research

14:30 4-2 **Characterization of Chalcogenide Selectors for Crossbar Switch Used in Nonvolatile FPGA**

Hideaki Numata[1], Naoki Banno[1], Koichiro Okamoto[1], Noriyuki Iguchi[1], Hiromitsu Hada[1], Masanori Hashimoto[2], Tadahiko Sugibayashi[1], Toshitsugu Sakamoto[1], Munehiro Tada[1]

[1]NEC Corp, [2]Osaka University

14:50 4-3 **Switching Current of Ta_2O_5 Based Resistive Analog Memories**

Yuanlin Li[1], Atsushi Tsurumaki-Fukuchi[1], Masashi Arita[1], Yasuo Takahashi[1], Takashi Morie[2]

[1]*Hokkaido University,* [2]*Kyushu Institute of Technology*

15:10 4-4 **Application of Extreme Value Theory to Statistical Analyses of Worst Case SRAM Data Retention Voltage**
Tomoko Mizutani, Kiyoshi Takeuchi, Takuya Saraya, Masaharu Kobayashi, Toshiro Hiramoto
The University of Tokyo

15:30 Break

Session 5: 3D NAND

Session Chair: Jiezhi Chen, *Shangdong University*

15:45 5-1 **Effect of Device Scaling on Lateral Migration Mechanism of Electrons in V-NAND**
Changbeom Woo, Shinkeun Kim, Jaeyeol Park, Hyungcheol Shin
Seoul National University

16:05 5-2 **Error Correction for Read-hot Data in 3D-TLC NAND Flash by Read-disturb Modeled Artificial Neural Network Coupled LDPC ECC**
Daiki Kojima, Toshiki Nakamura, Ken Takeuchi
University of Chuo

16:25 5-3 **Less Reliable Page Error Reduction for 3D-TLC NAND Flash Memories with Data Overhead Reduction by 40% and Data-retention Time Increase by 5.0x**
Kyosuke Maeda, Kyoji Mizoguchi, Ken Takeuchi
University of Chuo

Session 6: Posters

16:45-18:30

Session Co-Chairs: Katsuhiro Tomioka, *Hokkaido University,* Toshifumi Irisawa*, AIST*

16:45 Short oral presentation (1 min each)

6-1 **Impacts of Remote Coulomb Scattering on Hole Mobility in Si p-MOSFFETs at Cryogenic Temperatures**
Xianle le Zhang, Pengying Chang, Gang Du, Xiaoyan Liu
Institute of Microelectronics, Peking University

6-2 **Structural Design of T-gate, Air-spacer Poly-Si TFTs for RF applications**
Yu-An Huang, Yu-Hsiang Yeh, Horng-Chih Lin, Pei-Wen Li
National Chiao Tung University

6-3 **Short-channel Effects and Sub-Surface Behavior in Bulk MOSFETs and Nanoscale DG-SOI- MOSFETs: A TCAD Investigation**
Aditya Sankar Medury, Harshit Kansal
Indian Institute of Science Education and Research Bhopal

6-4 **Investigation of Ferroelectric Granularity for Double-Gate Negative-Capacitance FETs Considering Position and Number Fluctuations**

Che-Lun Fan, Kuei-Yang Tseng, You-Sheng Liu, Pin Su

National Chiao Tung University

6-5 **Characterization and Analysis of 5 nm-thick $Hf_{0.5}Zr_{0.5}O_2$ for Negative Capacitance FinFET**

Pin-Jui Chen[1], Meng-Ju Tsai[1], Fu-Ju Hou[2], Yung-Chun Wu[1]

[1]National Tsing Hua University, [2]Taiwan Semiconductor Research Institute

6-6 **Reduced RTN Amplitude and Single Trap induced Variation for Ferroelectric FinFET by Substrate Doping Optimization**

Zih-Tang Lin, Vita Pi-Ho Hu

University of National Central

6-7 **Negative Capacitance in Short-Channel Tunnel Field-Effect Transistors** Hung-Jin Teng[1,2], Yu-Hsuan Chen[1,2], Nguyen Dang Chien[3], Chun-Hsing Shih[1]

[1]National Chi Nan University, [2]National Tsing Hua University, [3]Dalat University

6-8 **Elastic Response of 10-nm Insulator Films Measured by Dynamic Indentation for Nano-scale Electron Device Fabrication**

Leonid Bolotov, Noriyuki Uchida, Wen Hsin Chang, Tatsuro Maeda, Shinji Migita

National Institute of Advanced Industrial Science and Technology

6-9 **ON Current Enhancement by Gate Controlled Strain in The InAs n-Type Piezoelectric Tunnel FETs**

Yuxiong Long[1], Jun Z Huang[2], Zhongming Wei[1], Jun-Wei Luo[1], Xiangwei Jiang[1]

[1]Institute of Semiconductors, CAS, [2]MaxLinear Inc.

6-10 **Ge Condensation Process for High ON/OFF Ratio of SiGe Gate-All-Around Nanowire Tunnel Field-Effect Transistor**

Ryoongbin Lee[1], Junil Lee[1], Sangwan Kim[2], Kitae Lee[1], Sihyun Kim[1], Soyoun Kim1, Yunho Choi1, Byung-Gook Park1

[1]Seoul National University, [2]Ajou University

6-11 **Effect of Fluorine Incorporation with HfO_2/Ti-GeO_x gate stack on p-Germanium Substrate through CF4 plasma treatment**

Yi He Tsai[1], Chen Han Chou1, Wen Kuan Yeh[2], Yu Hsien Lin[3], Fu Hsiang Ko[1], Chao Hsin Chien[1]

[1]University of National Chiao Tung, [2]Institute of Taiwan Semiconductor Research, [3]University of National United

6-12 **Feasibility of Ge double quantum dots with high symmetry and tunability in size and inter-dot spacing**

Kang-Ping Peng, Tsung-Lin Huang, Thomas George, Horng-Chih Lin, Pei-WEN Li Li

National Chiao Tung University

6-13 **The Preliminary Investigation of Octrafluorocyclobutane Plasma Jet Etching of Crystalline Silicon**

Chun Huang, Wei-Ting Liu, Wei-Lun Li, Li-Ko Huang, Yi-An Chen

Yuan Ze University

6-14 **Metallic Source/Drain Ge-Based Charge-Trapping Memory Cells**

Yu-Hsuan Chen[1,2], Chun-Hsing Shih[1], Hung-Jin Teng[1,2], Chenhsin Lien[2]

[1]National Chi Nan University, [2]National Tsing Hua University

6-15 **Modeling of Lateral Migration Mechanism of Holes in 3D NAND Flash Memory Charge Trap Layer during Retention Operation**

Jaeyeol park, Hyungcheol Shin

Seoul National University

6-16 **Prediction of Characteristics of Future Scaled 3D NAND Flash Memory by Using TCAD and SPICE**

Minsoo Kim, Hyungcheol Shin

Seoul National University

6-17 **Improved Gradual Reset Phenomenon in SiN_x-based RRAM by Diode-Connected Structure**

Min-Hwi Kim[1], Suhyun Bang[1], Tae-Hyeon Kim[1], Dong Keun Lee[1], Sungjun Kim[2], Seongjae Cho[3], Byung-Gook Park[1]

[1]Seoul National University, [2]Chungbuk National University, [3]Gachon University

6-18 **Effect of TiO Film Thickness on Resistive Switching Behavior of TiN/TiO_x/HfO_2/Pt RRAM Device**

Xiangxiang Ding, Lifeng Liu, Yulin Feng, Peng Huang

Peking University

6-19 **Comparison of switching characteristics of HfO_x RRAM device with different switching layer thicknesses**

Dong Keun Lee[1], Min-Hwi Kim[1], Suhyun Bang[1], Tae-Hyeon Kim[1], Yeon-Joon Choi[1], Sungjun Kim[2], Seongjae Cho[3], Byung-Gook Park[1]

[1]Seoul National University, [2]Chungbuk National University, [3]Gachon University

6-20 **Charge Effects on Semiconductor-Metal Phase Transition in Mono-layer $MoTe_2$**

Jixuan Wu[1,2], Xiaolei Ma[1,2], Jiezhi Chen[1], Xiangwei Jiang[2]

[1]Shandong University, [2]Chinese Academy of Science

6-21 **Design of learning circuit for single-electron neural networks**

Masaki Ueno, Takahide Oya

Yokohama National University

6-22 **Thermal-noise-harnessing single-electron memory pair circuit and its application to full adder circuit with simple structure**
Risa Kaide, Takahide Oya
Yokohama National University

6-23 **Design of multi-layer single-electron information-processing circuit mimicking behavior of bubble film for solving nonlinear problem**
Nobuhiko Kurata, Takahide Oya
Yokohama National University

6-24 **Single-electron Information-processing Circuit Mimicking Behavior of Fish Shoals**
Hideto Yamashita, Takahide Oya
Yokohama National University

6-25 **A Systematic Model Parameter Extraction using Differential Evolution Searching**
Jeesoo Chang, Min-Hye Oh1, Byung-Gook Park
Seoul National University

6-26 **Resonant Photocurrent at 1550 nm in an Erbium Low-Doped Silicon Transistor at Room Temperature**
Enrico Prati[1], Michele Celebrano[2], Lavinia Ghirardini[2], Marco Finazzi[2], Giorgio Ferrari[2], Takahiro Shinada[3], Keinan Gi[4], Yuki Chiba[4], Ayman Abdelghafar[4], Maasa Yano[4], Takashi Tanii[4]
[1]Consiglio Nazionale delle Ricerche, [2]Politecnico di Milano, [3]Tohoku University, [4]Waseda University

6-27 **Evaluation of Photosensitive Performance of Different Structured UTBB MOSFET**
Liqiao Liu, Xiaoyan Liu, Gang Du
Peking University

6-28 **Potential of Nano-scale Optical Rotor Based on a pn-Junction Wire** Yasuhisa Omura
Kansai University

Monday, June 10, 2019

Session 7: 2D materials

Session Chair: Iuliana Radu, *IMEC*

8:30 7-1 **[Invited] 3D Heterogeneous Integration with 2D Materials**
Eric Pop, Connor McClellan, Connor Bailey, Isha Datye, Alexander Gabourie, Ryan Grady, Kirstin Schauble, and Sam Vaziri
Stanford University

9:00 7-2 **Comparative study of high-k dielectric on MoS_2 deposited by plasma enhanced ALD**
Wenhsin Chang[1], Naoya Okada[1], Hidehiro Asai[1], Koichi Fukuda[1], Mitsuhiro Okada[1], Takahiko Endo[2], Yasumitsu Miyata[2], Toshifumi Irisawa[1]
[1]National Institute of Advanced Science and Technology, [2]Tokyo Metropolitan University

9:20 7-3 **Atomistic Study of Transport Characteristics in Sub-1nm Ultra-narrow Molybdenum Disulfide (MoS_2) Nanoribbon Field Effect Transistors**
Fei Wang[1,2], Xiaolei Ma[1,2], Jixuan Wu[1,2], Jiezhi Chen[1], Xiangwei Jiang[2]
[1]Shandong University, [2]Chinese Academy of Science

9:40 7-4 **Subthreshold Degradation of 2D material Junctionless FETs -Impact of Fringe Field from Source/Drain Electrodes through Insulator-**
Hidehiro Asai, Wen Hsin Chang, Naoya Okada, Koichi Fukuda, Toshifumi Irisawa
National Institute of Advanced Industrial Science and Technology

10:00 Break

Session 8: Ferroelectric FETs

Session Chair: Masaharu Kobayashi, *The University of Tokyo*

10:20 8-1 **Experimental Demonstration of Performance Enhancement of MFMIS and MFIS for 5-nm × 12.5-nm Poly-Si Nanowire Gate-All-Around Negative Capacitance FETs Featuring Seed-Layer and PMA-Free Process**
Shen-Yang Lee, Han-Wei Chen, Chiuan-Huei Shen, Po-Yi Kuo, Chun-Chih Chung, Yu-En Huang, Hsin-Yu Chen, Tien-Sheng Chao
National Chiao Tung University

10:40 8-2 **Study of Germanium Nanosheet Channel with Negative Capacitance Field-Effect-Transistor**
Yu Ning Chen[1], Fu Ju Hou[2], Chun Jung Su[2], Yung Chun Wu[1]
[1]National Tsing Hua Univerty, [2]Taiwan Semiconductor Research Institute

11:00 8-3 **Atomic-level Analysis by Synchrotron Radiation and Characterization of 2 nm, 3 nm, and 5 nm-thick $Hf_{0.5}Zr_{0.5}O_2$ Negative Capacitance FinFET**

Meng-Ju Tsai[1], Pin-Jui Chen[1], Po-Yang Peng[2], Fu-Ju Hou[3], Yung-Chun Wu[1]
[1]National Tsing Hua University, [2]National Synchrotron Radiation Research Center, [3]Taiwan Semiconductor Research Institute

11:20 8-4 **The Understanding of Gate Capacitance Matching on Achieving a High Performance NC MOSFET with Sufficient Mobility**
C. K. Chiang[1], P. Hsuan[1], Y. C. Luo[1], F. L. Li[2], E. R. Hsieh[1], C. H. Liu[2], Steve Chung[1]
[1]National Chiao Tung University, [2]National Taiwan Normal University

11:40 8-5 **Evaluation of Analog Circuit Performance for Ferroelectric SOI MOSFETs considering Interface Trap Charges and Gate Length Variations**
Yi-Chun Lu, Vita Pi-Ho Hu
University of National Central

12:00 Lunch

Session 9: Quantum Computing and Quantum Dots

Session Chair: Louis Hutin, *Leti*

13:30 9-1 **[Invited] Moving Spins from Lab to Fab: A Silicon-Based Platform for Quantum Computing Device Technologies**
Bogdan Govoreanu
IMEC

14:00 9-2 **Simultaneous operation of singlet-triplet qubits**
Federico Fedele, Anasua Chatterjee, Ferdinand Kuemmeth
University of Copenhagen

14:20 9-3 **Characterization of top-gated Si/SiGe devices for spin qubit applications**
Fabio Ansaloni, Christian Volk, Anasua Chatterjee, Ferdinand Kuemmeth
University of Copenhagen

14:40 9-4 **Dopant-Induced Terahertz Resonance of a Dopant-Rich Silicon Quantum Dot**
Takuya Okamoto[1,2], Naoki Fujimura[1,2], Tetsuo Kodera[2], Yukio Kawano[1,2]
[1]FIRST, Tokyo Institute of Technology, [2]Dept. of E.E., Tokyo Institute of Technology

15:00 9-5 **Si Surface Orientation Dependence of SiC Nano-Dot Formation in Hot-C Ion Implanted Bulk-Si Substrate**
Tomohisa Mizuno[1], Masaki Yamamoto[1], Takashi Aoki[1], Toshiyuki Sameshima[2]
[1]Kanagawa University, [2]Tokyo University of Agriculture and Technology

15:20 Break

Session 10: SOI-Based Novel Devices and RTN

Session Chair: Daniel Moraru, *Shizuoka University*

15:35 10-1 **Si Electron Nano-Aspirator towards Emerging Hydro-Electronics**

Manjakavahoaka Razanoelina[1], Himma Firdaus[2], Yasuo Takahashi[3], Akira Fujiwara[4], Yukinori Ono[1,2]

[1]Res. Inst. of Electronics, Shizuoka University, [2]Graduate School of Sci. and Tech., Shizuoka University, [3]Hokkaido University, [4]NTT Basic Research Laboratory

15:55 10-2 **Comparative Study on 1-THz Antenna-Coupled Bolometer with Various SOI-CMOS based Temperature Sensors: MOSFET, Diode, Resistor and Thermocouple**

Durgadevi Elamaran[1], Takeo Ueta[2], Hiroaki Satoh[2,3], Norihisa Hiromoto[1,2], Hiroshi Inokawa[1,3]

[1]Graduate School of Science and Technology, Shizuoka University, [2]Graduated School of Integrated Science and Technology, Shizuoka University, [3]Research Institute of Electronics, Shizuoka University

16:15 10-3 **Directivity of SOI Photodiode with Gold Surface Plasmon Antenna**

Anitharaj Nagarajan[1], Shusuke Hara[1], Hiroaki Satoh[1], Aruna Priya Panchanathan[2], Hiroshi Inokawa[1]

[1]Shizuoka University, [2]SRMIST

16:35 10-4 **Characterization of Four-Level Random Telegraph Noise in a Gate-All-Around Poly-Si Nanowire Transistor**

You-Tai Chang, Pei-Wen Li, Horng-Chih Lin

National Chiao Tung University

16:55 10-5 **From Gate Oxide Characterization to TCAD Predictions: Exploring Impact of Defects Across Technologies**

Gerhard Rzepa, Franz Schanovsky, Markus Karner

Global TCAD Solutions GmbH

17:15 **Closing Remarks**