Silicon Nanoelectronics Workshop 2023 (SNW 2023)

June 11th-12th, 2023
Rihga Royal Hotel Kyoto, Kyoto, Japan

Sunday, June 11th, 2023

8:45 Opening remarks
Katsuhiro Tomioka, *Hokkaido Univ.*

Session 1: Plenary
Session Chair: Katsuhiro Tomioka, *Hokkaido Univ.*

8:50 1-01 (Plenary)
CMOS Device Scaling by Nanosheet Channel Architectures and New Channel Materials
*Naoto Horiguchi, *imec (Belgium)*

9:20 1-02 (Plenary)
ALD Nanometer-Thin In_2O_3 for BEOL Logic, Memory and RF Applications
*Peide Ye, *Purdue Univ. (USA)*

Session 2: Machine Learning
Session Chair: Woo Young Choi, *Seoul National University*

9:50 2-01
Data Matching Engine for Efficient Big Data Searching Systems Using a RRAM Based Novel Computing Paradigm
Shiyue Song[1,2], Yizhou Zhang[1,2], Jin Kang[3], Kai Zheng, Weihai Bu[3], Lifeng Liu[1,2], Xiaoyan Liu[1,2], Jinfeng Kang[1,2], Peng Huang[1,2] ,[1]Peking Univ. (China), [2]Beijing Advanced Innovation Center for Integrated Circuits (China), [3]Semiconductor Technology Innovation Center (Beijing) Corp. (China)*

10:10 2-02
A Novel Ferroelectric Tunnel FET-based Time-Domain Content Addressable Memory with High Distance-Metric Linearity and Energy Efficiency for Edge Machine Learning
Weikai Xu[1], Jin Luo[1], Qianqian Huang[1], Ru Huang[1] ,[1]Peking University (China)*

10:30 2-03
Machine Learning-based Accurate Single Wafer Wet Etching Amount Prediction
*Shinsei Yoshikiyo[1], Hiroshi Horiguchi[2], Chihiro Matsui[1], Ken Takeuchi[1], *[1]Univ. of Tokyo (Japan), [2] SCREEN Semiconductor Solutions (Japan)*

Break (10 min)

Session 3: Neuromorphic Application I

Session Chair: Steve Chung, *National Yang Ming Chiao Tung Univ.*

11:00 3-01 (Invited talk)

Bayesian Nanoelectronics

*Damien Querlioz, *Université Paris-Saclay (France)*

11:30 3-02

Suppressed Relaxation Effect in TPT-RAM and Dual-mode Neural Network Application

*Xing Mou[1], Xiangpeng Liang[1], Yingjie Lyu[2], Jianshi Tang[1], Bin Gao[1], Pu Yu[2], He Qian[1], Huaqiang Wu[1], *[1]School of Integrated Circuits, Tsinghua University (China), [2]State Key Laboratory of Low Dimensional Quantum Physics and Department of Physics, Tsinghua University (China)*

11:50 3-03

Synapse Array with Buried Bottom Gate Structure for Neuromorphic Systems

*Bosung Jeon[1], Taejin Jang[1], Seongjae Cho[2], Hyungcheol Shin[1], Woo Young Choi[1], *[1]Seoul National Univ. (Korea), [2]Ewha Womans Univ. (Korea)*

Lunch break (12:10-13:10)

Session 4: **Neuromorphic Application II**

Session Chair: Kasidit Toprasertpong, *the Univ. of Tokyo*

13:10 4-01 (Invited talk)

In-Materio Reservoir Devices Made of Random Network of Nanomaterials for Application to Smart Sensors and Autonomous Robotics

*Hirofumi Tanaka, *Kyusyu Institute of Tech. (Japan)*

13:40 4-02

FDSOI-based 1T Pixel with Long-term Data Retention for *in-situ* Convolution

*Haozhang Yang[1], Zheng Zhou[1], Guihai Yu[1], Ruiqi Chen[1], Lixia Han[1], Peng Huang[1], Xiaoyan Liu[1], Jinfeng Kang[1], *[1]Peking Univ. (China)*

14:00 4-03

Artificial Nociceptor Based on Short-Term Memory TFT with Controllable Sensitization Level

*Ruiqi Chen[1,2], Ruiyi Li[1,2], Haozhang Yang[1,2], Guihai Yu[1,2], Yizhou Zhang[1,2], Yiyang Chen[1,2], Lianliang Wu[1,2], Junchen Dong[3], Dedong Han[1,2], Zheng Zhou[1,2], Peng Huang[1,2], Xiaoyan Liu[1,2], Jinfeng Kang[1,2], *[1]School of Integrated Circuits, Peking University (China), [2]Beijing Advanced Innovation Center for Integrated Circuits (China), [3]Beijing Information Science & Technology University (China)*

Break (10 min)

Session 5: Advanced CMOS Technology

Session Chairs: Masaharu Kobayashi, *Univ. of Tokyo*, Peide Ye, *Purdue Univ.*

14:30 5-01

High Performance Ge FinFET CMOS Invertor with I_{ON}=2.0 mA/μm at V_{OV} =1V, S.S.=64 mV/dec,

I_{ON}/I_{OFF}=2.5x10^6, and Voltage Gain=90 V/V by Using High Pressure Supercritical Fluid Hydroxide Oxidation

*Cheng-Yu Wu[1], Dun-Bao Ruan[2], Kuei-Shu Chang-Liao[1], Yao-Jen Lee[3], Yu-Chuan Chiu[4], Chih-Wei Liu[1], Guan-Ting Liu[1], Bo-Lien Kuo[1], Kai-Chun Yang[1], Cheng-Han Li[1], Po-Tsun Liu[4], *[1]National Tsing Hua University (Taiwan), [2]Fuzhou University (China), [3]Taiwan Semiconductor Research Institute (Taiwan), [4]National Yang Ming Chiao Tung University (Taiwan)*

14:50 5-02

Enhanced Performance for SiGe/Si Gate-All-Around Field-Effect-Transistor with Ge Condensation Using Supercritical Fluid Treatment

*Wei-Ren Chen[1], Dun-Bao Ruan[2], Kuei-Shu Chang-Liao[1], Hao-Yan Wang[1], Guang-Li Luo[3], Yu-Chuan Chiu[4], Ting-Kai Kuan[1], Po-Tsun Liu[4], *[1]National Tsing Hua University (Taiwan), [2]Fuzhou University (China), [3]Taiwan Semiconductor Research Institute (Taiwan), [4]National Yang Ming Chiao Tung University (Taiwan)*

15:10 5-03

Thermal consideration in nanoscale gate-all-around vertical transistors

*Guilhem Larrieu[1], Houssem Rezgui[2], Abhishek Kumar[1], Jonas Müller[1], Sylvain Pelloquin[1], Yifan Wang[2], Marina Deng[2], Aurélie Lecestre[1], Cristell Maneux[2], Chhandak Mukherjee[2], *[1]LAAS-CNRS (France), [2]IMS laboratory (France)*

15:30 5-04

Thermal and Performance Analysis of Back-side Power Delivery Network beyond 3nm Technology Node

*Haoyu Zhang[1], Linlin Cai[1], Yutao Chen[1], Jianwen Lin[1], Wangyong Chen[1], *[1]Sun Yat-Sen Univ. (China)*

15:50 5-05

Green Laser Crystallized Poly-Si Thin-film Transistor and CMOS Inverter using HfO_2-ZrO_2 Superlattice Gate Insulator and Microwave Annealing for BEOL Applications

*Chih-Hsiang Chang[1], Siao-Cheng Yan[1], Chong-Jhe Sun[1], Ming-Yueh Huang[1], Bo-An Chen[1], Xin-Chan Zhong[1], Yi-Wen Lin[1], Yung-Chun Wu[1], *[1]National Tsing Hua Univ. (Taiwan)*

16:10 5-06

Study of Ferroelectric HfO_2-ZrO_2 Superlattice Poly-Si Junctionless Nanosheet Gate-all-around Field-effect-transistor and CMOS Inverter

*Xin-Chan Zhong[1], Siao-Cheng Yan[1], Ming-Yueh Huang[1], Chih-Siang Chang[1], Chong-Jhe Sun[1], Bo-An Chen[1], Yi-Wen Lin[1], Yung-Chun Wu[1], *[1]National Tsing Hua University (Taiwan)*

Session 6: Poster presentation (poster short presentation 16:40~17:00)

Session Chair: Kuniyuki Kakushima, *Tokyo Tech.*

17:00-18:30 at Syunjyu II

Monday, June 12th, 2023

Session 7: Si Nanoelectronics & Device Physics

Session Chair: Takahide Oya, *Yokohama National Univ.*

8:50 7-01 (invited talk)

Silicon Electron Nano-Aspirator - Current enhancement based on electron-electron scattering –

*Yukinori Ono, *Shizuoka Univ. (Japan)*

9:20 7-02

Effects of Quantum Confinement on Charge-Based Threshold Voltage Definition

*Kiyoshi Takeuchi[1], Masaharu Kobayashi[1], Toshiro Hiramoto[1], *[1]Univ. of Tokyo (Japan)*

9:40 7-03

An Enhanced AC Conductance Method with Source/Drain Resistance Correction for Self-Heating Effects of Novel Nano-Scaled Devices

*Jyun-Yan Kuo[1], Wei Lee[1], Ke-Wei Su[1], Chung-Kai Lin[1], *[1]Taiwan Semiconductor Manufacturing Company (Taiwan)*

10:00 7-04

Drag of Electron-Hole Bilayer in Silicon-on-Insulator at Low Temperature

*Ahmed Nabil[1], Manjakavahoaka Razanoelina[1], Masahiro Hori [1], Akira Fujiwara[2], Yukinori Ono[1], *[1]Shizuoka Univ. (Japan), [2]NTT Basic Research Laboratory (Japan)*

10:20 7-05

Modification and Ablation of Thin Silicon-on-Insulator Films by fs-Laser

*Daniel Moraru[1,2], Tsutomu Kaneko[1], Daniel Smith[2], Tomas Katkus[2], Soon Hock Ng[2], Saulius Juodkazis[2], *[1]Shizuoka Univ. (Japan), [2]Swinburne Univ. of Tech. (Australia)*

Break (10 min)

Session 8: Quantum dots

Session Chair: Pei-Wen Li, *National Yang Ming Chiao Tung Univ.*

10:50 8-01 Integrable Germanium Few-Hole Double Quantum-Dots and Single-Hole Transistors using CMOS Fabrication Approaches

*Chi-Cheng Lai[1], I-Hsiang Wang[1], Ting Tsai[1], Horng-Chih Lin[1], Pei-Wen Li[1], *[1]National Yang Ming Chiao Tung University (Taiwan)*

11:10 8-02 Single-Electron Charge Sensor Self-Aligned to a Quantum Dot Array by Double-Gate Patterning Process for a Large-Scale Silicon Quantum Computer

*Takuma Kuno[1], Takeru Utsugi[1], Ryuta Tsuchiya[1], Noriyuki Lee[1], Gou Shinkai[1], Toshiyuki Mine[1], Itaru Yanagi[1], Raisei Mizokuchi[2], Jun Yoneda[2], Tetsuo Kodera[2], Shinichi Saito[1], Digh Hisamoto[1], Hiroyuki Mizuno[1], *[1]Hitachi, Ltd. (Japan), [2]Tokyo Institute of Technology (Japan)*

11:30 8-03 Individual Control of Characteristics of Vertically Stacked Silicon Quantum Dots

*Junoh Kim[1], Tomoko Mizutani[1], Takuya Saraya[1], Hiroshi Oka[2], Takahiro Mori[2], Masaharu Kobayashi[1,3], Toshiro Hiramoto[1], *[1]IIS, Univ. of Tokyo (Japan), [2]AIST (Japan), [3]d.lab, Univ. of Tokyo (Japan)*

11:50 8-04 Structural and Electrostatic Confinement of a Single Electron in a Scalable 2D Array

of Quantum Dots

*Amina Sadik[1], Etienne Nowak[1], Louis Hutin[1], Pierre-André Mortemousque[1], Benoit Bertrand[1], *[1]CEA-Leti, Univ. of Grenoble Alpes (France)*

Lunch break (12:10-13:10)

Session 9: Application of 2D material

Session Chair: Daniel Moraru, *Shizuoka, Univ.*

13:10 9-01 (invited talk)

Graphene Based NEMS and Electric Field Sensor: From Research to Real-World Applications

*Afsal Kareekunnan[1], Manoharan Muruganathan[1], Ngoc Huynh Van[1], Marek E Schmidt[1], Takeshi Kudo[2], Takeshi Maruyama[2], Hiroshi Mizuta[1,3], *[1]JAIST (Japan), [2]Otowa Elec. (Japan), [3]Univ. Southampton (UK)*

13:40 9-02

Novel MoS_2 Dual-Gate FET with a Highly Scaled EOT of ~2.4 nm High-k Gate Dielectric Layer for Reconfigurable Logic Gate and High-Precision Analog Synapse

*Lingqi Li[1], Haofei Zheng[1], Heng Xiang[1], Yu-Chieh Chien[1], Kah-Wee Ang[1,2], *[1]Department of Electrical and Computer Eng., National Univ. of Singapore (Singapore), [2]Inst. of Materials Res. and Eng., A*STAR (Singapore)*

14:00 9-03

Forming-Free Resistive Switching by Lateral Ag Ion Migration on MoS_2

*Sofia Cruces[1], Lukas Voelkel[1], Jimin Lee[1], Dennis Braun[1], Ardeshir Esteki[1], Annika Grundmann[2], Holger Kalisch[2], Michael Heuken[2,3], Andrei Vescan[2], Alwin Daus[1], Max Christian Lemme[1,4], *[1]Chair of Electronic Devices, RWTH Aachen Univ. (Germany), [2]Compound Semiconductor Tech., RWTH Aachen Univ. (Germany), [3]AIXTRON SE (Germany), [4]AMO GmbH (Germany)*

14:20 9-04

Scalability of h-BN Based Memristors: Yield and Variability Considerations

Abdelrahman S. Abdelrahman[1], Hesham ElSawy[2], Mario Lanza[3], Deji Akinwande[4], *Feras Al-Dirini[1,5], *[1]Electrical Engineering Department, King Fahd University of Petroleum & Minerals (Saudi Arabia), [2]School of Computing, Queen's University (Canada), [3]Physical Science and Engineering Division, King Abdullah University of Science and Technology (Saudi Arabia), [4]Microelectronics Research Center, The University of Texas at Austin (United States of America), [5]Center for Advanced Materials, King Fahd University of Petroleum & Minerals (Saudi Arabia)*

Break (10 min)

Session 10: Memory Technology

Session Chairs: Minoru Oda, *KIOXIA Cooperation*

14:50 10-01

A 40-nm Loadless 4T-SRAM TRNG MACRO with Read-just-after-write (RAW) Scheme Featuring 5.3Gb/s and 3.64TOP/W

Y. S. Wu[1], K. H. Chang[1], P. S. Huang[1], M. L. Miu[1], S. Y. Huang[1], S. M. Lu[1], H. S. Su[1], *E Ray Hsieh[1], *[1]National Central University (Taiwan)*

15:10 10-02

Record-High Memory Window and Robust Retention Anti-Fuse OTP Memory: Electrical and Reliability Characteristics

Dong Ru Hsieh[1], *Jia Chian Ni[1], Wei Ju Yeh[1], Tzu Chieh Hong[1], Zi Yang Hong[1], Yan Kui Liang[1], Huai En Luo[1], Michael Hsu[1], Ta Chun Cho[2], Tien Sheng Chao[1], *[1]National Yang Ming Chiao Tung Univ. (Taiwan), [2]Taiwan Semiconductor Res. Inst. (Taiwan)*

15:30 10-03

Physical Understanding on the Anti-fuse Instability to Construct a Selector-Type One-Time-Programming Memory in the High-k Metal-Gate CMOS Generation

C. C. Chuang[1], C. W. Chang[1], H. W. Chen[1], *T. C. Kao[1], Y. J. Li[1], J. C. Guo[1], Steve S Chung[1], *[1]National Yang Ming Chiao Tung Univ. (Taiwan)*

15:50 10-04

Physical mechanisms and Enhancement of Endurance Degradation of SiO_x: Ag-based Volatile Memristors

*Ruiyi Li[1,2], Haozhang Yang[1,2], Yizhou Zhang[1,2], Xujin Song[1,2], Nan Tang[1,2], Ruiqi Chen[1,2], Zheng Zhou[1,2], Weihai Bu[3], Kai Zheng[3], Jin Kang[3], Lifeng Liu[1,2], Jinfeng Kang[1,2], Peng Huang[1,2], *[1]Peking University (China), [2]Beijing Advanced Innovation Center for Integrated Circuits (China), [3]Semiconductor Technology Innovation Center (Beijing) Corporation (China)*

16:10 10-05

Stand-alone STT-MRAM development on VCT transistor in 0.0045 μm² unit cell

Jaewoo Kim[1], *Qiong Tuo[1], Handong Xu[1], Yali Tan[1], Tingting Gu[1], Haiyang Dong[1], Xingkun Xue[1], Zelun Li[1], Kuoming Huang[1], Zhonghan Cao[1], Bowen Dong[2], Kaifeng Dong[3], Huihui Li[2], Chao Zhao[2], Abraham Yoo[1], *[1]ChangXin Memory Tech., Inc. (China), [2]Superstring Academy of Memory Tech. (China), [3]China Univ. of Geosciences (China)*

Break (10 min)

Session 11: Ferroelectric devices

Session Chairs: Katsuhiko Nishiguchi, *NTT Basic Research laboratories*

16:40 11-01 (invited talk)

Stacked Gate-All-Around Nanosheet Channel Ferroelectric $Hf_xZr_{1-x}O_2$ FETs With NH_3 Plasma Treatment Featuring High Footprint Current

Dong-Ru Hsieh, Chia-Chin Lee, *Tien-Sheng Chao, National Yang Ming Chiao Tung University *(Taiwan)*

17:10 11-02

New Insights into the Memory Window Estimation in FeFET from a Dynamic Perspective

*Puyang Cai[1], Hao Li[1], Chang Su[1], Tianxiang Zhu[1], Lining Zhang[1], Runsheng Wang[1], Ru Huang[1], *[1]Peking University (China)*

17:30 11-03

Investigation of HfO_2/ZrO_2 Superlattice Dielectric and High-*k* AlON Interfacial Layer on Ferroelectric FinFET

*Ming-Yueh Huang[1], Siao-Cheng Yan[1], Xin-Chan Zhong[1], Chih-Siang Chang[1], Chong-Jhe Sun[1], Bo-An Chen[1], Yi-Wen Lin[1], Yung-Chun Wu[1], *[1]National Tsing Hua Univ. (Taiwan)*

17:50 11-04

Vertically Stacked Ge Diamond-shape Nanowires GAAFET with Ferroelectric HZO

*Bo-An Chen[1], Yi-Wen Lin[1], Hao-Hsiang Chang[1], Chih-Hsiang Chang[1], Ming-Yueh Huang[1], Xin-Chan Zhong[1], Siao-Cheng Yan[1], Chong-Jhe Sun[1], Fu-Ju Hou[2], Yung-Chun Wu[1], *[1]National Tsing Hua Univ. (Taiwan), [2]Taiwan Semiconductor Research Inst. (Taiwan)*

18:10 Closing remarks Kuniyuki Kakushima, *Tokyo Tech.*

Poster Presentation (June 11th, 17:00-18:30, with poster short presentation 16:40~17:00)

P01

Performance Improvement of Single-Electron Reservoir Computing Circuit with Multiple-Tunnel-Junction Single Electron Oscillator

*Shunya Watanabe[1], Takahide Oya[1], *[1]Yokohama National Univ. (Japan)*

P02

Single-Electron Information-Processing Circuit Inspired by Principles of Molecular Computing

*Kairi Yokoyama[1], Takahide Oya[1], *[1]Yokohama National Univ. (Japan)*

P03

Logically Synthesized Invertible Logic Based on Many-body Effects with Probabilistic-bit Implementation

*Yihan He[1], Chao Fang[1], Sheng Luo[1], Gengchiau Liang[1], *[1]National Univ. of Singapore (Singapore)*

P04

Influence of Weight Transfer Error on Vector-Matrix Multiplication Using AND Array Architectures

*Junsu Yu[1], Donghyun Ryu[1], Taejin Jang[1], Woo Young Choi[1], *[1]Seoul National Univ. (Korea)*

P05

Experimental Demonstration of Memristor Delay-Based Logic In-Memory Ternary Neural Network

Adrien Renaudineau[1], Kamel-Eddine Harabi[1], Clément Turck[1], Axel Laborieux[1], Elisa Vianello[2], Marc Boquet[3], Jean-Michel Portal[3], *Damien Querlioz[1], *[1]Univ. Paris-Saclay, CNRS, C2N (France), [2]CEA-LETI, Univ. Grenoble-Alpes (France), [3]Aix-Marseille Univ., CNRS, IM2NP (France)*

P06

A Crossbar-wise IR-drop Compensation Schemes for 5G/6G Hybrid Precoding with Highly-parallel Analog RRAM Array

*Qi Qin[1], Qingtian Zhang[1], Bin Gao[1], Jianshi Tang[1], He Qian[1], Huaqiang Wu[1], *[1]Tsinghua Univ. (China)*

P07

Ultra-Large Memory Window of 3.8V and 75% Read/Write Speed Improvement through Stressed Alumina and Angstrom-Laminated $HfZrO_2$

*Zi-Rong Huang[1], Sheng Min Wang[1], Cheng Rui Liu[1], Yu Ting Chen[1], Yu Tzu Cai[1], Zheng Kai Chen[1], Chia Shou Pai[1], Ying Tsan Tang[1], *[1]National Central Univ. (Taiwan)*

P08

Optimization of Ferroelectricity in Al-Doped HfO_2 Capacitors: Electrical and Endurance Characteristics

*Dong Ru Hsieh[1], Huai En Luo[1], Jia Chian Ni[1], Zi Yang Hong[1], Yi Hsiu Chen[1], Wei Ju Yeh[1], Tien Sheng Chao[1], *[1] National Yang Ming Chiao Tung Univ. (Taiwan)*

P09

Improved Switching behaviors of MFM Capacitor with Reduced E_c and Enhanced P_r-V Linearity by Using La-Al co-doped HfO_2 Ferroelectric layer

*Xujin Song[1], Haolin Li[1], Zhuohua Tang[1], Peng Huang[1], Xiaoyan Liu[1], Jinfeng Kang[1], *[1]Peking Univ. (China)*

P10

Variability Analysis of Stacked-Nanosheet FeFET for MLC Memory and Synapse Applications

*Heng Li Lin[1], Pin Su[1], [1]*Univ. of National Yang Ming Chiao Tung (Taiwan)*

P11

New Understanding of Memory Window Reduction Induced by Ferroelectric Dynamics for HfO_2-based 1T1C FeRAM

*Zhiyuan Fu[1], Mengxuan Yang[1], Kaifeng Wang[1], Qianqian Huang[1,2,3], Ru Huang[1,2], [1]*Peking Univ. (China),* [2]*Beijing Advanced Innovation Center for Integrated Circuits (China),* [3]*Beijing Superstring Academy of Memory Tech. (China)*

P12

(Withdrawn) ~~Impact of Fringing Field on the Memory Window of FeFET~~

~~*Athira Sunil[1], Maximilian Lederer[1], Yannick Raffel[1], Franz Müller[1], Konrad Seidel[1], Thomas Kämpfe[1], Sourav De[1], [1]*Fraunhofer Institute for Photonic Microsystems (Germany)*~~

P13

Impact of Si-Based Interfacial Layer for Ferroelectric Memory

*Siddheswar Maikap[1,2], Asim Senapati[1], Zhao-Feng Lou[3], Min-Hung Lee[3], [1]*Chang Gung Univ. (Taiwan),* [2]*Keelung Chang Gung Memorial Hospital (Taiwan),* [3]*National Taiwan Normal Univ. (Taiwan)*

P14

(Withdrawn) ~~A Comprehensive Understanding for AFeFET with Double Hysteresis Loop Model: Guidelines for Performance and Reliability~~

~~*Min Liao[1], Junshuai Chai[1], Jinjuan Xiang[2], Kai Han[3], Yanrong Wang[4], Hao Xu[1], Xiaolei Wang[1], Jing Zhang[4], Wenwu Wang[1], [1]*Inst. of Microelectronics Chinese Academy of Sciences (China),* [2]*Beijing Superstring Academy of Memory Tech. (China),* [3]*Weifang Univ. (China),* [4]*North China Univ. of Tech. (China)*~~

P15

In-Solution Germanium Selenide Nanosheets as Charge Trapping Layer in Flash Memories

Nazek El-Atab[1], *Bashayr Ali Alqahtani[1], [1]*Program of Electrical and Computer Engineering, King Abdullah Univ. of Sci. and Tech. (Saudi Arabia)*

P16

Spherical Shallow Trench Isolation with silicon nitride layer in Buried Gate DRAM for reducing pass gate disturbance

*Yeon-Seok Kim[1,2], Chang-Young Lim[1,2], Min-Woo Kwon[1,2], [1]*National Univ. of Gangneung-Wonju (Korea),* [2]*Lab. of ISDL (Korea)*

P17

A Physics-based Numerical Model of Resistive Switching Behavior in Electrochemical Metallization Memristor

*Yeongkwon Kim[1], Byung Chul Jang[1], [1]*Kyungpook Nat'l Univ. (Korea)*

P18

A High-Speed and Self-calibratable True Random Number Generator (TRNG) based on Unified Selector-RRAM

*Yabo Qin[1], Zongwei Wang[1,2], Jiajun Gao[1], Linbo Shan[1], Qishen Wang[1], Yimao Cai[1,2], Ru Huang[1,2], [1]*Peking*

Univ. (China), [2]Beijing Adv. Innovation Center for IC (China)

P19

Generative Network Utilizing Random Number Based on Memristor Array for Medical Image Synthesis

*Namju Kim[1], Byung Chul Jang[1], *[1]Kyungpook Nat. Univ. (Korea)*

P20

Design of New Single-Electron Reaction-Diffusion Circuit with Ability to Generate and Control Plane Waves

*Keiichiro Tamura[1], Yuito Nakamori[1], Takahide Oya[1], *[1]Yokohama National Univ. (Japan)*

P21

Theoretical Study of High Performance Germanium Nanowire Quantum Dot

*Han-Wei Yang[1], Yung-Feng Wu[1], Ming-Jung Hsu[1], Shao-Chen Lee[1], Ying-Tsan Tang[1], *[1]National Central University (Taiwan)*

P22

Enhanced Electrical Performance of Ge nMOSFET with Rapid Remote Plasma Oxidation Treatment

*Jia-Cheng Liu[1], Dun-Bao Ruan[2], Kuei-Shu Chang-Liao[1], Guan-Ting Liu[1], [1]*National Tsing Hua University (Taiwan), [2]Fuzhou University (China)*

P23

Improved Radiation Hardness for Nanosheet FETs with Partial Bottom Dielectric Isolation

*Xun-Ting Zheng[1], Vita Pi-Ho Hu[1], *[1]National Taiwan University (Taiwan)*

P24

Phosphorus Deactivation and Electron Mobility Enhancement in Ultrathin Silicon Nanosheets

*Michele Perego[1], Andrea Pulici[1,2], Stefano Kuschlan[1,3], Gabriele Seguini[1], Fabiana Taglietti[2], Marco Fanciulli[1,2], Riccardo Chiarcos[3], Michele Laus[3], *[1]CNR-IMM Unit of Agrate (Italy), [2]Università degli Studi di Milano-Bicocca (Italy), [3]Università del Piemonte Orientale "A. Avogadro" (Italy)*

P25

Performance Investigation of Source/Drain Extension Region on Nanosheet FET: A Digital Design Perspective

*Shobhit Srivastava[1], Sourabh Panwar[1], Shashidhara M.[1], Navjeet Bagga[2], Deepak Joshi[1], Abhishek Acharya[1], *[1]Sardar Vallabhbhai National Institute of Technology, Surat, Gujarat (India), [2]IIT Bhubaneswar, Odisha (India)*

P26

Comprehensive Investigation of Back Gate Biasing on Performance of Line TFETs

*Sourabh Panwar[1], Shobhit Srivastava[1], Shashidhara M[1], Prabhat Dubey[2], Deepak Joshi[1], Abhishek Acharya[1], *[1]Sardar Vallabhbhai National Institute of Technology, SVNIT (India), [2]Univ. of Pisa (Italy)*

P27

Atomically Thin 0.65nm and 6nm Vertical Side-Wall MoS_2 Channel Transistors

*Kihan Kim[1], Byung Chul Jang[1], *[1]Kyungpook National Univ. (Korea)*