平成 19 年 8 月 10 日

応用物理学会北海道支部
会員各位

応用物理学会北海道支部

講演会のお知らせ

下記講演会を開催いたしますので、多数ご参加下さいますようご案内申し上げます。

演題：Room-temperature Functional Nanoelectronic Devices and Circuits with Branched Semiconductor Nanojunctions
講師：Hongqi Xu 氏
（Division of Solid State Physics, Lund University (Sweden), Professor）
日時：平成 19 年 8 月 20 日（月） 15:00～16:30
場所：北海道大学 量子集積エレクトロニクス研究センター セミナー室（3F、304 室）
共催：応用物理学会北海道支部 （共催団体：北海道大学量子集積エレクトロニクス研究センター）

講演の要旨
Present digital logic gates are primarily built from field effect transistors (FETs) such as complementary metal oxide semiconductors with the gate length in the deep sub-μm regime. As device feature sizes approach the nanometer regime, fundamental physical constraints and increasingly prohibitive economic costs will make further miniaturization in electronic circuits difficult, and this has motivated efforts worldwide to search for new strategies to meet expected computing demands of the future. In the strategy for device fabrication, bottom-up approaches to electronic devices with well-defined nanoscale building blocks have been demonstrated. An alternative strategy is to develop new device concepts by making a revolutionary departure from the FET-based paradigm. The approach must exploit the emerging inherent properties of nanostructures. Here I will review a paradigm based on multi-terminal junctions (MTJs), in which the novel properties of electron transport emerg
ed are exploited.

A MTJ is a nanostructure-compatible device formed from three or more coupled nonlinear conductors, such as quantum point contacts realizable by standard top-down nanofabrication method or a bottom-up approach. With top-down approach, various MTJ structures have been fabricated on high-quality semiconductor heterostructures and novel electrical properties of MTJs have been found. I will present our recent theoretical and experimental studies of these novel properties. As for applications, I will demonstrate that MTJs can be used as diodes and triodes, as well as a building block for analog and logic circuits. These devices and circuits function at room temperature, and the layout of the devices and circuits features fabrication by a single-step lithography process that is suitable for mass production with low-cost approaches such as nanoimprint lithography. Furthermore, the demonstrated device principles are shown to apply equally well to multi-terminal junctions made with bo
ttom-up approaches. As examples, recent work on nanoelectronic devices made from branched nanotubes and semiconductor nanowires will be reviewed.

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