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2012 Silicon Nanoelectronics Workshop

June 9-10, 2013

Rihga Royal Hotel Kyoto, Kyoto, Japan

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Sunday, June 9, 2013

8:30 **Opening Remarks**

Ken Uchida (Keio University)

Session 1: Plenary & Nonvolatile Memories

- 8:40 1-1 (Plenary) Fundamentals of redox-based resistive switching -materials, switching kinetics, and scaling potential of ReRAM devices, Rainer Waser^{1,2}, Stephan Menzel², Ilia Valov¹, and Eike Linn² (¹Forschungszentrum Jülich, ²RWTH Aachen University)
- 9:10 1-2 Insights into the Voltage-time Dilemma of Metal Oxide-based RRAM for High Speed and Low Voltage AC Switching, P. Huang, Y. J. Wang, B. Gao, B. Chen, F. F. Zhang, L. Zeng, G. Du, J. F. Kang, and X. Y. Liu (Peking University)
- 9:30 1-3 Analysis of Data Retention Time-to-Failure in Charge Trap NAND Flash Memories, Byeong-In Choe^{1,2}, Wandong Kim¹, Jung-Kyu Lee¹, Byung-Gook Park¹, and Jong-Ho Lee¹ (¹Seoul National University, ²Samsung Electronics)
- 9:50 1-4 An Optimum Asymmetric Coding Strategy to Improve Program-Disturb Error in 2X, 3X and 4Xnm NAND Flash Memories for Highly Reliable Enterprise Solid-State Drives (SSDs) Masafumi Doi¹, Shuhei Tanakamaru^{1, 2} and Ken Takeuchi¹ (¹Chuo University, ²University of Tokyo)
- 10:10 1-5 Comparative Study of TiN Metal Gate and Poly-Si Gate Charge-Trapping Type FinFET Flash Memories, Y. X. Liu, T. Matsukawa, K. Endo, S. O'uchi, J. Tsukada, H. Yamauchi, Y. Ishikawa, W. Mizubayashi, Y. Morita, S. Migita, H. Ota, and M. Masahara (AIST)
- 10:30 1-6 Pi-Gate Tunneling Field-Effect Transistor Charge Trapping Nonvolatile Memory, Hsin-Yi Lin, Yi-Ruei Jhan, Min-Feng Hung and Yung-Chun Wu (National Tsing Hua University)

10:50 Break

Session 2: Ge Channel MOSFET

- 11:15 2-1 Effectiveness of Quasi-Confinement Technology for Improving P-Channel Si and Ge MOSFET Performance, Nuo Xu¹, Marek Hytha², Hideki Takeuchi², Xiangyang Huang², Robert J. Stephenson², Nattapol Damrongplasit¹, Nyles Cody², Robert J. Mears², Tsu-Jae King Liu¹ (¹UC Berkeley, ²Mears Technologies)
- 11:35 2-2 Ultrathin EOT and High Mobility Ge pMOSFETs by in-situ H₂O Plasma Grown GeO₂ and HfON Gate Dielectric, Li-Jung Liu, Kuei-Shu Chang-Liao, Chung-Hao Fu, Ting-Ching Chen, Chen-Chien Li, Jen-Wei Cheng, Chun-Chang Lu, Tzu-Min Lee, Li-Ting Chen, Shih-Han Yi, Sheng-Kai Chen, Tien-Ko Wang (National Tsing Hua University)
- 11:55 2-3 Ultra-thin GeO₂ Formation by Oxygen Radicals (O*) for Advanced Ge Gate Stacks - Reaction kinetics, film quality and MIS characteristics -, W. J. Song, W. F. Zhang, C. H. Lee, T. Nishimura, and A. Toriumi (University of Tokyo)

12:05 Lunch

Session 3: Nanoscale FETs: Small & Low Power

- 13:30 3-1 (Invited) MOSFET Scaling to 3-nm-Long and 1-nm-Thick Channel, Shinji Migita, Yukinori Morita, Meishoku Masahara, and Hiroyuki Ota (AIST)
- 14:00 3-2 Experimental Determination of the Ballistic Transport Parameters in Nanoscale Trigate CMOS Devices, T. C. Lin¹, E. R. Hsieh¹, Steve S. Chung¹, C. H. Tsai², R. M. Huang², and C. T. Tsai² (¹National Chiao Tung University, ²United Microelectronics Corporation)
- 14:20 3-3 Impact of Drain-Induced Barrier Lowering on Ultra-Low Supply Voltage CMOS Circuits Operating in Subthreshold Region, Seung-Min Jung, Tomoko Mizutani, and Toshiro Hiramoto (University of Tokyo)
- 14:40 3-4 Evaluation of Interface State Density of Strained-Si MOS Interfaces by Conductance Method, W.-L. Cai, M. Takenaka and S. Takagi (University of Tokyo)

15:00 Break

Session 4: Nanoscale FETs: Device Model & Variability

- 15:15 4-1 (Invited) Graphene and Beyond-Graphene 2D-Crystals for Green Electronics, Kaustav Banerjee (UCSB)

- 15:45 4-2 Reduced Cell Current Variability in Fully Depleted Silicon-on-Thin-BOX (SOTB) SRAM Cells at Supply Voltage of 0.4V, T. Mizutani¹, Y. Yamamoto², H. Makiyama², H. Shinohara², T. Iwamatsu², H. Oda², N. Sugii², and T. Hiramoto¹ (¹University of Tokyo, ²LEAP)
- 16:05 4-3 SRAM Cell Stability Parameter: Noise Margin or Vmin?, Anil Kumar¹, Takuya Saraya¹, Shinji Miyano², and Toshiro Hiramoto¹ (¹University of Tokyo, ²STARC)
- 16:25 4-2 Variability and Recovery Behaviors of |V_{th}| Shift of pFETs by High-Voltage OFF-State and ON-State Stress for Post-Fabrication SRAM Cell Stability Self-Improvement, Nurul Ezaila Alias¹, Anil Kumar¹, Takuya Saraya¹, Shinji Miyano², and Toshiro Hiramoto¹ (¹University of Tokyo, ²STARC)

Session 5: Posters

16:45-18:30 Starting with Short Oral Presentation

- 5-1 Exploring the Size Limit of RRAM Cross Point Array: Optimization of Device Characteristics and Bias Schemes, Yexin Deng, Peng Huang, Bing Chen, Bin Gao, Xiaoyan Liu, Jinfeng Kang (Peking University)
- 5-2 Improved uniformity of HfOx based resistive switching device by inserting AlOx near TiN top electrode, Y. Hou, B. Chen, B. Gao, L. F. Liu, D. D. Han*, Y. Wang, X. Y. Liu, J. F. Kang, X. Zhang (Peking University)
- 5-3 Modeling of Unipolar Resistive Switching of Pt/TiO₂/Pt Capacitor, Yusuke Kondo and Yasuhisa Omura (Kansai University)
- 5-4 Investigation of Three Dimensional NAND Flash Memory Based on Gate Stacked ARray (GSTAR), Do-Bin Kim, Yoon Kim, Se Hwan Park, Wandong Kim, Joo Yun Seo, Seung-Hyun Kim, and Byung-Gook Park (Seoul National University)
- 5-5 High Speed and Good Retention of Ω -Gate P-channel Twin Poly-Si Thin Film Transistors EEPROM, Mu-Shih Yeh*, Kuan-Cheng Liu, Min-Feng Hung, and Yung-Chun Wu (National Tsing Hua University)
- 5-6 Comparison of High-Temperature Performance between Junctionless and Conventional Poly-Si Thin-Film Transistors, Nan-Heng Lu¹, Yung-Chun Wu¹, Hung-Bin Chen², Ya-Chi Cheng¹, Jun-Ji Su¹ and Ming-Hung Han² (¹National Tsing Hua University, ²National Chiao-Tung University)
- 5-7 Performance of p-Type Junctionless Poly-Si Thin-Film Transistors with Raised S/D, Jun-Ji Su¹, Ya-Chi Cheng¹, Nan-Heng Lu¹, Yung-Chun Wu¹, and Hung-Bin Chen² (¹National Tsing Hua University, ²National Chiao-Tung University)

- 5-8 Fabrication and Characterization of a Short-channel Tri-gated Poly-Silicon Thin-Film Transistor, Ko-Hui Lee¹, Horng-Chih Lin^{1,2} and Tiao-Yuan Huang¹ (¹National Chiao-Tung University, ²National Nano Device Laboratories)
- 5-9 Back-Gate Biasing Influence on the Electron Mobility and the Threshold Voltage of Ultra Thin Box Multigate MOSFETs, F. G. Ruiz, E. G. Marín, A. Godoy, I. M. Tienda-Luna, C. Martínez-Blanco, F. Gámiz (Universidad de Granada)
- 5-10 Characteristics of trapezoidal shaped channel for Junctionless Bulk FinFETs, Ya-Chi Cheng¹, Hung-Bin Chen², Ming-Hung Han², Yung-Chun Wu¹, Nan-Heng Lu¹, and Jun-Ji Su¹ (¹National Tsing Hua University, ²National Chiao-Tung University)
- 5-11 Impacts of Sidewall Inclination on the Characteristics of Bulk Fin FET, L. Shen, Z. Y. Lun, G. Du, X. Zhang, X. Y. Liu (Peking University)
- 5-12 Correlation between Random Interface Traps and Dopants in 22nm High-k/Metal gate Junctionless FinFETs, Yijiao Wang, Kangliang Wei, Lang Zeng, Xiaoyan Liu*, Gang Du, Jinfeng Kang (Peking University)
- 5-13 Analog Characteristics of Junctionless Bulk Transistor, Ming-Hung Han¹, Shiang-Shiou Yen^{1,2}, Hung-Bin Chen^{1,2}, Yung-Chun Wu², and Chun-Yen Chang¹ (¹National Chiao-Tung University, ²National Tsing Hua University)
- 5-14 Improving Subthreshold Slope of Silicon Nanowire Tunneling FET Using Microwave Dopant Activation, Shiang-Shiou Yen^{1,2}, Yu-Long Wang², Min-Feng Hung², Yung-Chun Wu², and Chun-Yen Chang¹ (¹National Chiao-Tung University, ²National Tsing Hua University)
- 5-15 Characteristics of Asymmetry-Gate Tunneling Field-Effect Transistor, Yi-Ruei Jhan, Min-Feng Hung and Yung-Chun Wu (National Tsing Hua University)
- 5-16 Mixed-mode Analysis of Different Mode Si Nanowire Transistors Based Circuit, Juncheng Wang, Gang Du*, Kangliang Wei, Lang Zeng, Xiaoyan Liu (Peking University)
- 5-17 High Drain Bias Simulations of Random Dopant and Metal Gate Workfunction Variability in a 50nm gate length In_{0.53}Ga_{0.47}As GAA MOSFET, N. Seoane¹, G. Indalecio², E. Comesana², A. J. García-Loureiro², M. Aldegunde¹ and K. Kalna¹ (¹Swansea University, ²University of Santiago de Compostela)
- 5-18 Investigation of 2-D Quantum Confinement Effect on DIBL for Multi-Gate n-MOSFETs with InGaAs Channel, Shu-Hua Wu, Yu-Sheng Wu, and Pin Su (National Chiao Tung University)
- 5-19 Quantum simulations of Si and Ge p-type double-gate MOSFETs: influence of phonon-scattering, channel length and orientation, E. Dib, M. Bescond, N. Cavassilas, F. Michelini and M. Lannoo (UMR CNRS)

- 5-20 Positive Bias Temperature Instability of n-Channel MOSFET with High-k Gate Dielectric after Ionizing Radiation Exposure, Bing-Yue Tsui¹, Ming-Hung Sun¹, Ting-Ting Su¹, Bor-Yuan Shew², and Yang-Tung Huang¹ (¹National Chiao Tung University, ²National Synchrotron Radiation Research Center)
- 5-21 NEGF Computational study of Advanced Nanoscale FET Biosensors for Single DNA Molecule Detection, Aryan Afzalian, and Denis Flandre (Université Catholique de Louvain)
- 5-22 Correlated Fano effect in Silicon Nanowire Transistors, H. Mera¹, Y. M. Niquet², M. Bescond¹, and M. Lannoo¹ (¹IM2NP-UMR CNRS, ²INAC/SP2M/Lsim)
- 5-23 Doped silicon quantum dots in high magnetic fields, F. Gonzalez-Zalba¹, J. Galibert², D. A. Williams¹, and T. Ferrus¹ (¹Hitachi Cambridge Laboratory, ²Laboratoire National des Champs Magnétiques Intenses)
- 5-24 Excited states of double-gate Si single-electron transistors in the few electron regime, I. Yoshioka¹, T. Uchida¹, M. Arita¹, A. Fujiwara², and Y. Takahashi¹ (¹Hokkaido University, ²NTT Basic Research Laboratories)
- 5-25 DC characteristics of a two isolated double quantum dot structure in silicon, S. Das, T.-Y. Yang, A. Betz, F. Gonzalez-Zalba, T. Ferrus and D. A. Williams (Hitachi Cambridge Laboratory)
- 5-26 Simulation of charge-based qubit dynamics in silicon double quantum dots, J. Mosakowski¹, T. Ferrus², D. A. Williams², A. Andreev² and C. H. W. Barnes¹ (¹Cavendish Laboratory, ²Hitachi Cambridge Laboratory)

Monday, June 10, 2013

Session 6: Nano Wire FETs & Formation

- 8:30 6-1 (Invited) III-V nanowire channels on Si: vertical FET applications, Katsuhiko Tomioka and Takashi Fukui (Hokkaido University)
- 9:00 6-2 Vertically grown germanium nanowire diodes on silicon and germanium substrates, Nishant Chandra¹, Clarence J. Tracy¹, Stephen M. Goodnick¹, Jeong-Hyun Cho², S. Tom Picraux³ (¹Arizona State University, ²University of Minnesota, ³Los Alamos National Laboratory)
- 9:20 6-3 Anisotropy in Surface Self-Diffusion on Si Nanowires and Its Impact on Wire Instability in Hydrogen Annealing, Naoya Morioka^a, Jun Suda, and Tsunenobu Kimoto (Kyoto University)
- 9:40 6-4 Modeling Surface-Roughness-Induced Scattering in Non-Planar Silicon Nanostructures, Z. Stanojević and H. Kosina (TU Wien)
- 10:00 Break

Session 7: Single-Electron & Dopant Phenomena

- 10:15 7-1 The coupled atom transistor: a first realization with shallow donors implanted in a trigate silicon nanowire, B. Voisin¹, B. Roche¹, E. Dupont-Ferrier¹, B. Sklénard^{2,3}, M. Cobian⁴, X. Jehl¹, O. Cueto², R. Wacquez², M. Vinet², Y-M. Niquet⁴, S. De Franceschi¹ and M. Sanquer¹ (¹CEA-INAC-SPSMS, ²CEA-LETI Minatoc, ³STMicroelectronics, and ⁴CEA-INAC-SP2M)
- 10:35 7-2 Fabrication and characterisation of down-scaled multi-configuration Silicon quantum dot devices, Y. P. Lin¹, J. I. Perez-Barraza², M. K. Husain¹, F. M. Alkhalil¹, Y. Tsuchiya¹, N. Lambert², D. A. Williams³, A. J. Ferguson², H. M. H. Chong¹ and H. Mizuta^{1,4} (¹University of Southampton, ²Cavendish Laboratory, ³Hitachi Cambridge Laboratory, ⁴JAIST)
- 10:55 7-3 Double-dot Si single-electron transistor with tunable coupling capacitance by the number of electrons in the dot, Takafumi Uchida¹, Hiroto Takenaka¹, Isamu Yoshioka¹, Masashi Arita¹, Akira Fujiwara², and Yasuo Takahashi¹ (¹Hokkaido University, ²NTT Basic Research Laboratories)
- 11:15 7-4 Electrical characteristics of donor-induced quantum dots formed in nanoscale selectively-doped SOI-FETs, D. Moraru, A. Samanta, Y. Kuzuya, T. Nagasaka, T. Mizuno, and M. Tabe (Shizuoka University)

11:35 7-5 Dopant-Induced Random Telegraph Signal in Nanoscale pn and pin Junctions, Sri Purwiyanti^{1,2}, Roland Nowak^{1,3}, Daniel Moraru¹, Takeshi Mizuno¹, Ryszard Jablonski³, Djoko Hartanto³, and Michiharu Tabe¹ (¹Shizuoka University, ³Universitas Indonesia, ³Warsaw Univ. of Technology)

11:55 Lunch

Session 8: Emerging Devices

13:30 8-1 (Invited): H. Sunamura, K. Kaneko, N. Inoue, N. Furutake, S. Saito, M. Narihiro, N. Ikarashi, J. Kawahara, M. Hane, and Y. Hayashi (Renesas Electronics)

14:00 8-2 Shape-Engineered Antenna-Coupled Thermocouples for Infrared Detection, Gergo P. Szakmany¹, Clemens Preiss², Alexei O. Orlov¹, Gary H. Bernstein¹, and Wolfgang Porod¹ (¹University of Notre Dame, ²University of the German Federal Armed Forces Munich.)

14:20 8-3 Refractive Index Measurement by SOI Photodiode with Gold Surface Plasmon, Antenna, Hiroaki Satoh, Shohei Iwata, Ken Kawakubo, Atsushi Ono, and Hiroshi Inokawa (Shizuoka University)

14:40 8-4 Direct helium ion milling technology: towards the fabrication of extremely down-scaled graphene nanodevices, Shuojin Hang¹, Zakaria Moktadir¹, Nima Khalor¹, Shinichi Saito¹ and Hiroshi Mizuta^{1,2} (¹University of Southampton, ²JAIST)

15:00 8-5 Integrate-and-Fire Neuron CMOS Circuit with a Multi-input Floating body MOSFET, Min-Woo Kwon, Hyungjin Kim, Jungjin Park, Jong-Ho Lee, Hyungcheol Shin, and Byung-Gook Park (Seoul National University)

15:20 8-6 Sustained Nano-Mechanical Oscillation of a Resonant-Body Transistor by Frequency-Modulated Heterodyne Phase-Locked-Loop, S.T. Bartsch, A. Rusu, A.M. Ionescu (Swiss Federal Institute of Technology EPFL)

15:40 Break

Session 9: Rump Session

15:55-17:00

Subject: BEOL Devices and New Applications

Moderator: Toshitsugu Sakamoto (LEAP)

Panelists: