2013 Silicon Nanoelectronics Workshop

Call for Papers

June 9-10, 2013, Rihga Royal Hotel Kyoto, Kyoto, Japan
(held prior to VLSI Technology Symposium, Satellite Workshop of VLSI Symposia)
Sponsored by the Japan Society of Applied Physics and the IEEE Electron Device Society

Deadline for Abstracts: March 27, 2013

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General Information

The 2013 Silicon Nanoelectronics Workshop will be held at Rihga Royal Hotel Kyoto, Japan on June 9-10, 2013, just prior to VLSI Symposium on Technology as a satellite workshop of the VLSI Symposia. The workshop will focus on silicon-related nanoelectronics to bridge a gap between the Si nano-technology and the "real" VLSI world. The first Silicon Nanoelectronics Workshop was held in June, 1996 at Honolulu, Hawaii, USA. The 2013 Silicon Nanoelectronics Workshop will be the 18th in a series of annual workshops.

Scope

The workshop will cover various aspects of VLSI-related silicon nanoelectronics. Areas of interest include, but are not limited to:

- Si based sub-10 nm FETs with conventional and novel architecture including vertical and multiple-gate devices and novel channel materials
- Device physics of Si based nanodevices including quantum effects, nonequilibrium and ballistic transport
- Si based nanoscale device modeling and simulations
- Extreme processing of Si based nanostructures, including nanopatterning
- Junction and insulator technology for Si based nanodevices
- Nanoscale surface, interface, and heterojunction effects in Si based devices
- Si based device scaling issues including doping fluctuations and atomic granularity
- Circuit design issues and novel circuit architectures for Si based nanodevices including silicon based quantum computing
- Optoelectronics using silicon nanostructures
- ***Nanoelectronics challenging to replace Si technologies (Graphene, CNTs, etc.)***

Submission of Abstract

Prospective authors are requested to submit a PDF file of the abstract ON-LINE at http://diana.pe.titech.ac.jp/~snw2013/

The abstract must consist of one page of text and one page of figures. The abstract must include the title, the author's names, affiliation, full address, phone and FAX numbers, and e-mail address. Faxed copies of the abstract will not be accepted. Accepted abstracts will be reproduced in the workbook exactly as received. The deadline for abstracts is **March 27, 2013**.
Questions may be addressed to **y-taka@nano.ist.hokudai.ac.jp** (Y. Takahashi).

Further Information

Registration forms and hotel reservation forms will be provided in the Web site of the 2013 VLSI Technology Symposium (http://www.vlsisymposium.org/). Some of the accepted papers will be presented in "Poster Sessions". Further information can be obtained at http://diana.pe.titech.ac.jp/~snw2013/

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